# Embedded Electronics in Solar Material (20-211)

#### Team:

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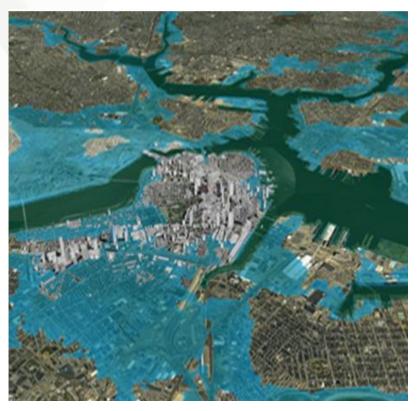
Sponsor: Glenn Weinreb (Manhattan 2)



#### Introduction

# The U.S Government predicts sea level rise within the next 60-200 years





This sample image of a sea level rise courtesy of Sea Level Rise Viewer [1]



This sample image of a sea level rise courtesy of Sea Level Rise Viewer [2]

#### **Client Background**

Manhattan 2 R&D To Create A Low-Carbon Society

Glenn Weinreb (Founder/CTO)

All work done is 100% open source and free

> The organization has an emphasis on renewable energy sources

Non-profit corporation aimed to reduce CO2 emissions energy sources

MA2

Logo and Profile picture courtesy of Manhattan 2 [5]

#### Problem

Solar panels can be an efficient solution to the energy crisis, but panels that are currently on the market can be bulky and expensive

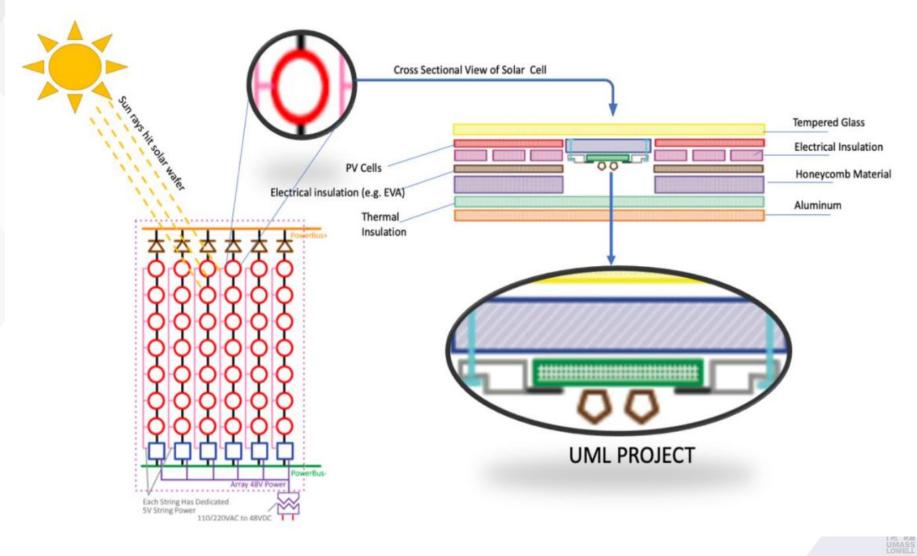


The above image of solar cell courtesy of expgreen [3]



The above image of solar cell courtesy of Energis Melbourne [4]

#### **Project Description**



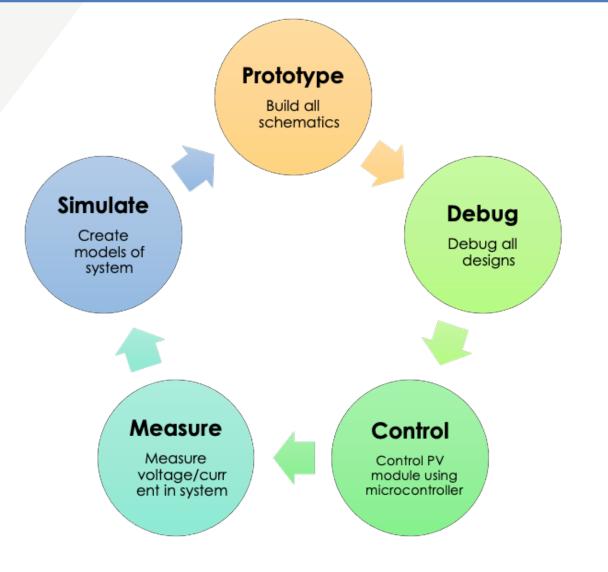
#### **Project Objective**

The team will prototype, test, and S improve the design of schematics provided by Manhattan 2 as well as develop a program that will A combine to create a 300 W DC to **DC converter for a flexible PV** R solar cell model by the end of Т May 2021.



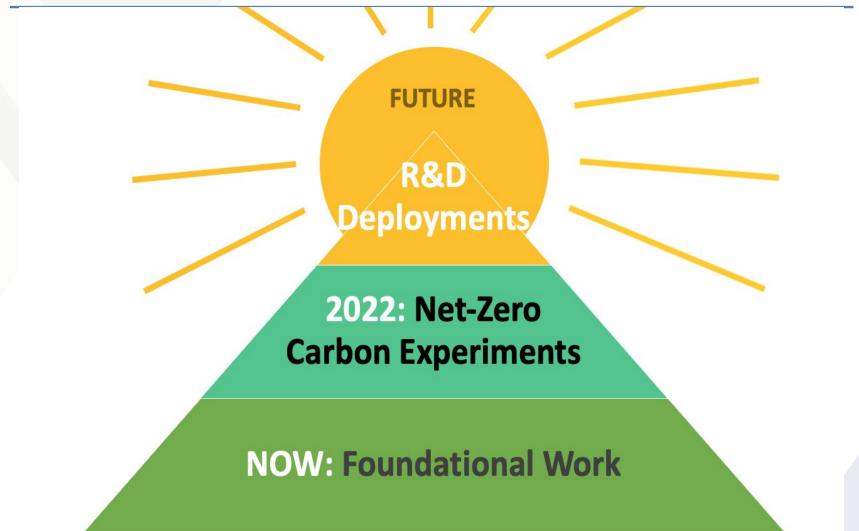
#### **Proposed Solution**







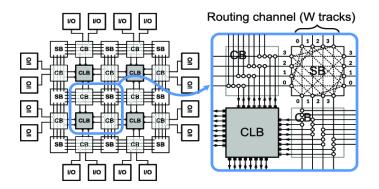
#### **Benefits**



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#### **Deliverables:** Summary

- FPGA SPI communication system
- Breadboards:
  - Power supplies
  - Voltage Reference
  - Voltage Measurement
  - Power Conversion
- 16-bit A/D conversion system
- Photovoltaic simulation models







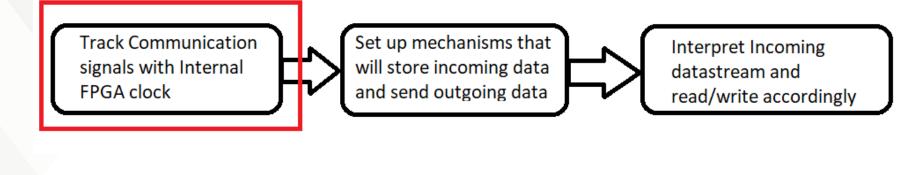
## Design: FPGA SPI System

#### **Communication System**

- Because Covid restrictions limited the ability to have all portions of the project in the same physical area, the communication system operation had to be confirmed using simulation software
- ActiveHDL was used to simulate the SPI communication Verilog code



#### Analysis: FPGA SPI System



Signal name	Value	•	•	•	160	•	•	•	176	•	•	•
JI _10Mhz_Clock	1 to 0	JUU	UU	UU	UU	UU	UU	Л	ПЛ	ПЛ	ЛЛ	ЛЛ
лг_SPI_SCK	0											
<pre>.rr _SPI_SCK_risingedge</pre>	0											
лг_SPI_SCK_fallingedge	0											



#### Analysis: FPGA SPI System

Track Communication signals with Internal FPGA clock Set up mechanisms that will store incoming data and send outgoing data

Interpret Incoming datastream and read/write accordingly

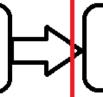
Signal name	Value	160 240 320 400 480 560
.rr_10Mhz_Clock	0 to 1	
ЛГ_SPI_SCK	1	
JU _SPI_MOSI	0	
JU _SPI_SSEL	1	
	84FF	X X X X X X X X X X 84FF
⊞ <b>л</b> r holdReg	84FF	хххх Х
Im registerAdressByteStream	0400	хххх Х
	00FF	хххх Х
JU write_inverseRead	1	

## Analysis: FPGA SPI System

Track Communication signals with Internal FPGA clock



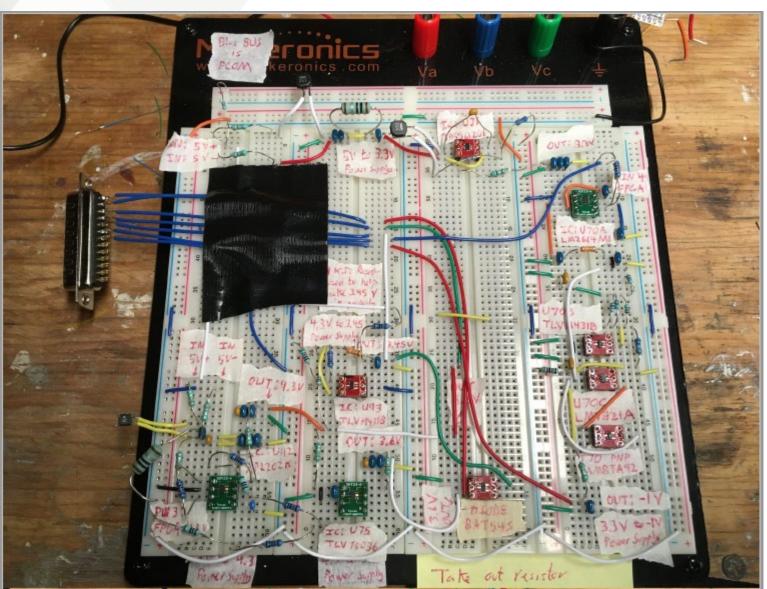
Set up mechanisms that will store incoming data and send outgoing data



Interpret Incoming datastream and read/write accordingly

Signal name	Value	· · · 80 · · · 160 · · · 240 · · · 320 · · · 400 · · · 480 · · · 560 · · · 640 · · · 720 · · · 800 · · · 880 · · · 960 · · · 1040 · ·
JU _SPI_SCK	0	<u> </u>
JU _SPI_MOSI	0	
JUT_SPI_SSEL	1	
JUL SPI_MISO	0	
JT XMC_PIN_P2_6	0	
JLT XMC_PIN_P2_5	0	
JT XMC_PIN_P0_11	0	
JT XMC_PIN_P0_10	0	
JT XMC_PIN_P0_8	0	
JT XMC_PIN_P0_6	0	
JUL XMC_PIN_P0_5	0	
JT XMC_PIN_P0_4	0	
Register 4		
	Me	ssage 1: Write all 1's to Register 4 Message 2: Write all 0's to Register 4

#### **Design:** Prototype Power Supplies

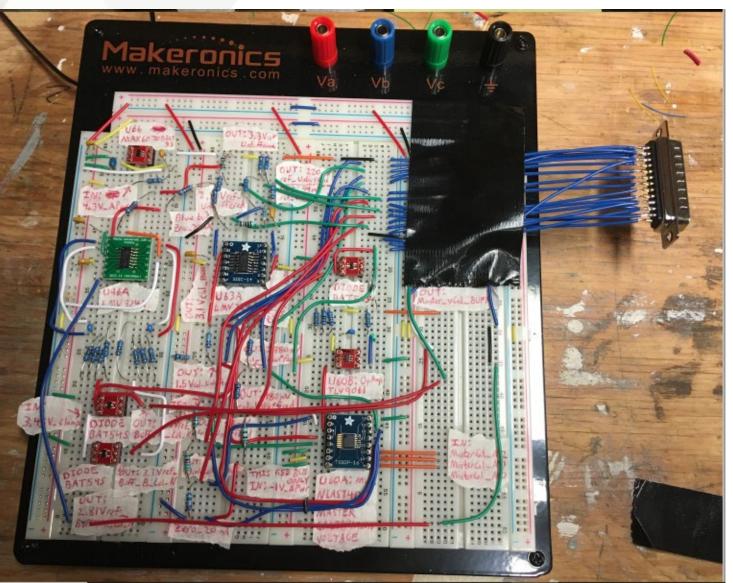


Power Supplies Breadboard with connector attaching to Vectorboard

> connecto r used to hook up between boards



#### **Design:** Prototype Voltage References

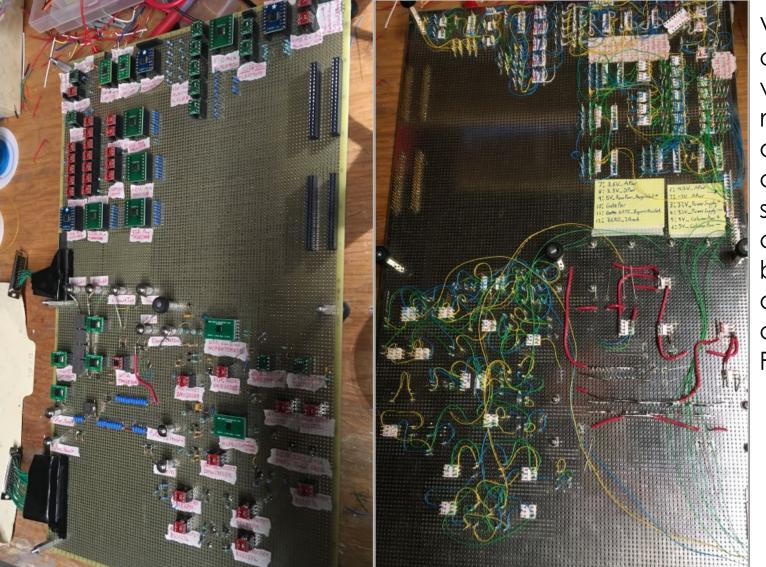


Voltage Reference Breadboard with connector attaching to Vectorboard

connector
used to hook
up between
boards



#### Design: Prototype Power Conversion & FPGA connectors & more

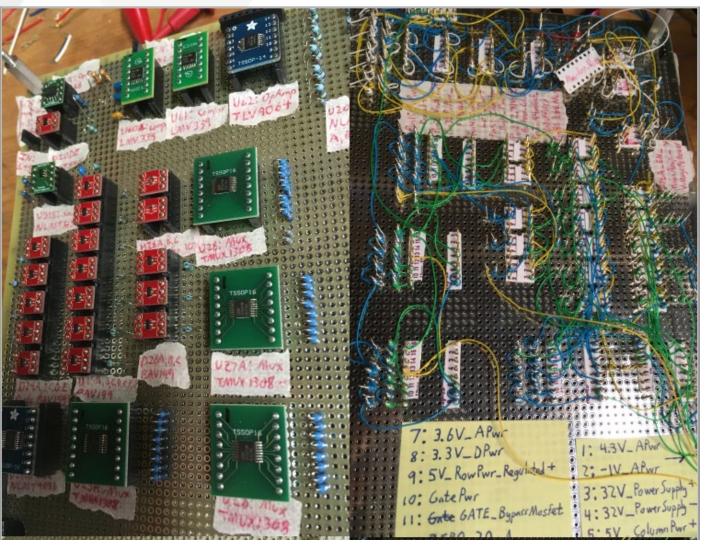


Vectorboard containing voltage measurement and power conversion schematics, connectors to breadboards, and connectors to FPGA

wirewrappingsoldering



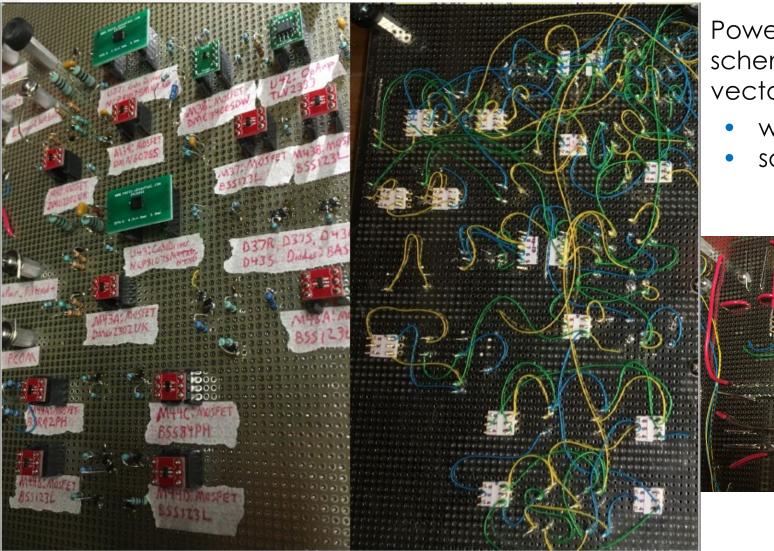
#### **Design: Prototype Voltage Measurement**



Voltage Measurement schematics on the vectorboard

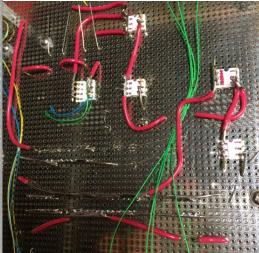
- wire wrapping
- soldering

#### **Design:** Power Conversion (cont'd)



Power Conversion schematics on the vectorboard

- wire wrapping
- soldering



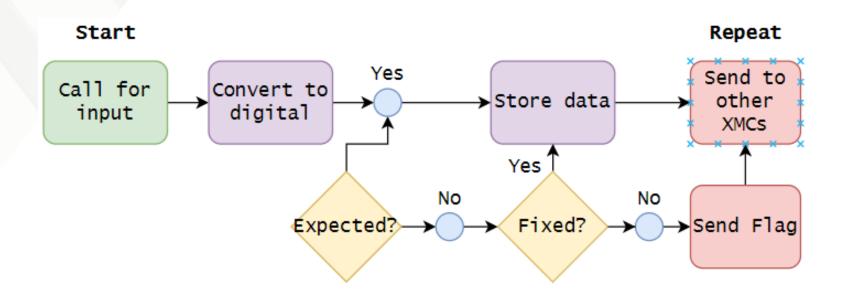
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#### Work Area



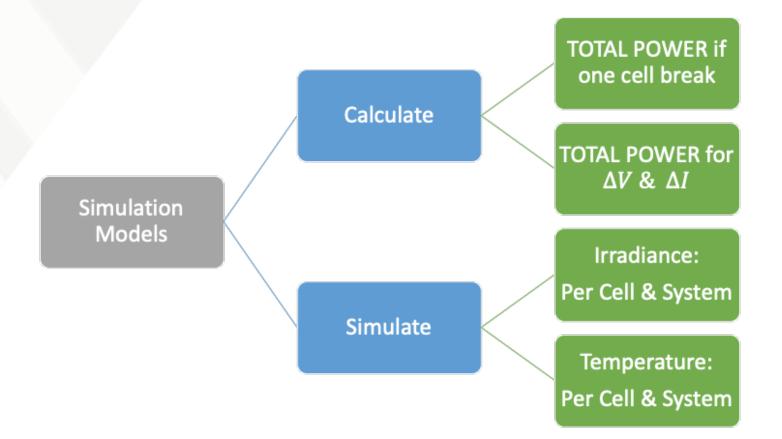
UMASS

A/D Design





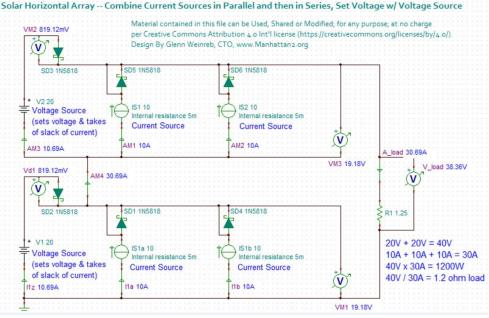
#### **Design: Simulations & Calculators**





#### **Design: Solar Array**

- The array used can be used in a larger scale when developing larger solar panels
- Each array contains 2 layer of variable components
  - One voltage source
  - Two current sources
- The array can be expanded into many different layers

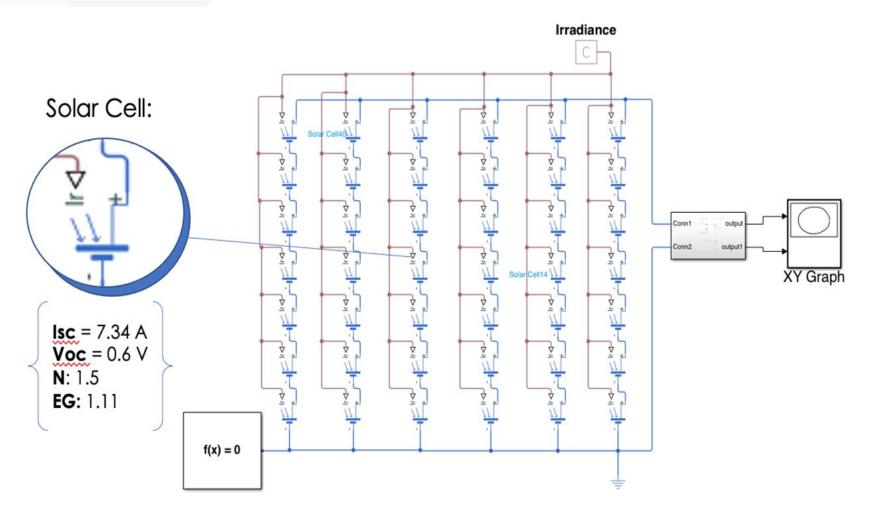


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[9] Courtesy of Manhattan2

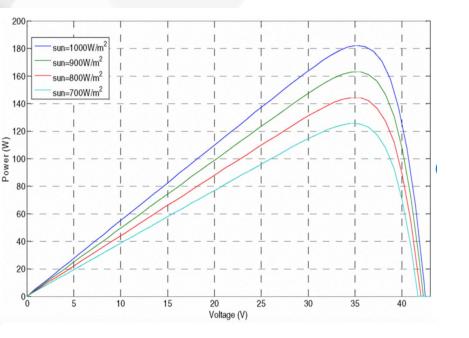


#### **Design: Irradiance Model**





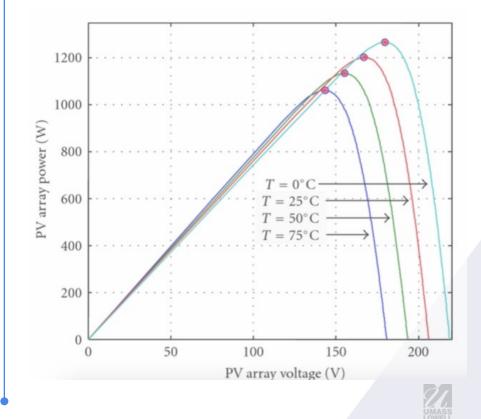
#### **Analysis:** Irradiance & Temperature



#### Factors for lower power yield:

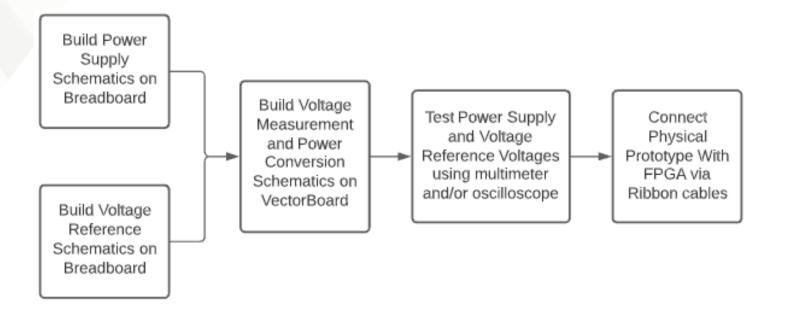
- Cloud Cover
- Air Pollution
- Time of Year
- Location Latitude

Nominal operating solar cell temperature is critical to solar cell performance



#### **Evaluation:** Prototyping Schematics

• One of the objectives was to physically prototype the circuit.





#### **Evaluation:** A/D Converter and Data Handling

- Successfully tested A/D converter.
- Measurement interval was timed
- Program tests for unwanted spikes and removes them from data.
- The system is ready to be used on the larger schematic.



## **Evaluation:** FPGA SPI Communication

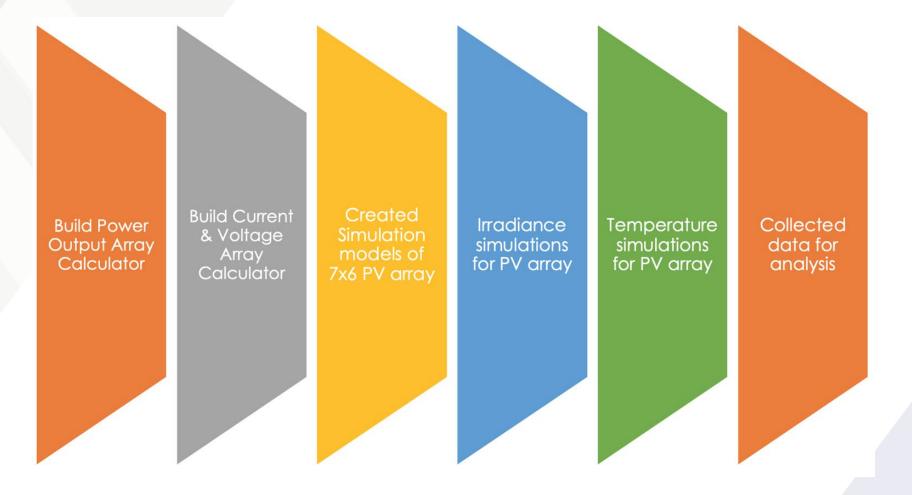
- Successful created SPI code for the FPGA that will enable communication with the microcontroller
- Allows for read/write operations as needed to each circuit input that is located on the Manhattan 2 solar cell schematic
- Simulation software was used to verify the correct operation of all communication elements
- This satisfies the requirements for this section of the project as defined in our original deliverables

#### **Evaluation:** Solar Array

- The objective was to create a simulated array circuit using Excel
- The Excel sheet was able to calculate total current, voltage, and power for each layer based on input values

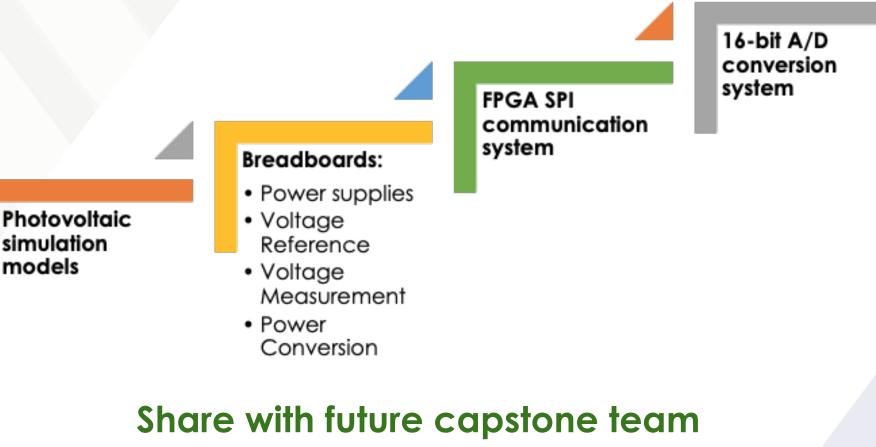
Layer	Voltage Sources (V)	Curren A (A)	Current B (A)	Total Current (A)	Total Power (W)
L1	10.0	3.0	0.5	3.5	35.0
L2	9.8	3.3	0.8	4.1	40.2
L3	9.4	3.5	0.9	4.4	41.4
L4	9.1	3.8	1.3	5.1	46.4
L5	8.6	4.0	1.5	5.5	47.3
L6	8.6	4.2	1.7	5.9	50.7
L7	7.9	4.5	2.0	6.5	51.4
L8	7.3	4.8	2.2	7.0	51.1
L9	7.0	2.4	2.6	5.0	35.0
L10	6.5	0.0	0.0	0.0	0.0

#### **Evaluation:** Simulation Models





#### **Evaluation:** Summary of all Parts





simulation

models

## Future Work (2021)

#### Finish the following schematics:

- Communication Network
- Fully connected circuit

#### Complete the following parts:

- CANbus omnidirectional communication
- Test for complete circuit operation and faults
- Print fully tested circuit board
- Plot voltage fluctuations
- Test power optimization



#### **SUMMARY & ACKNOWLEDGEMENT**

#### SUMMARY:

- 20-211 Team delivered critical foundational starting point of the proposed Manhattan2 project
- While challenges existed, the team overcome them and executed required deliverables with satisfactory outcome

#### ACKNOWLEDGEMENT: THANK YOU TEAM MANHATTAN2 AND PROF. SCHMID!



# **Thank You**

