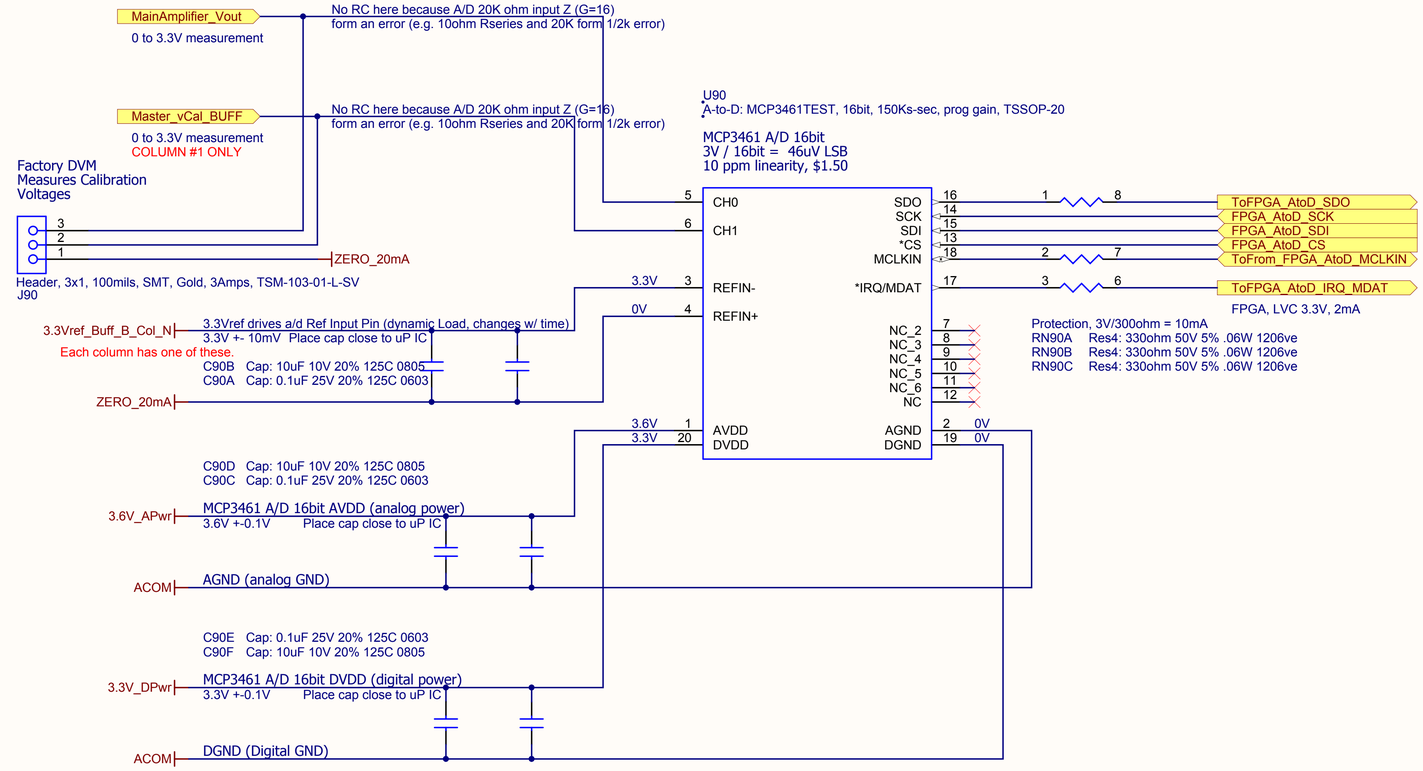
16bit A/D

ALL COLUMNS HAVE THIS



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DC-to-DC Converter, 24..84V Input, 10V/200mA/2W, Output (MOSFET Gate Power)

ALL COLUMNS HAVE THIS

SUMMARY

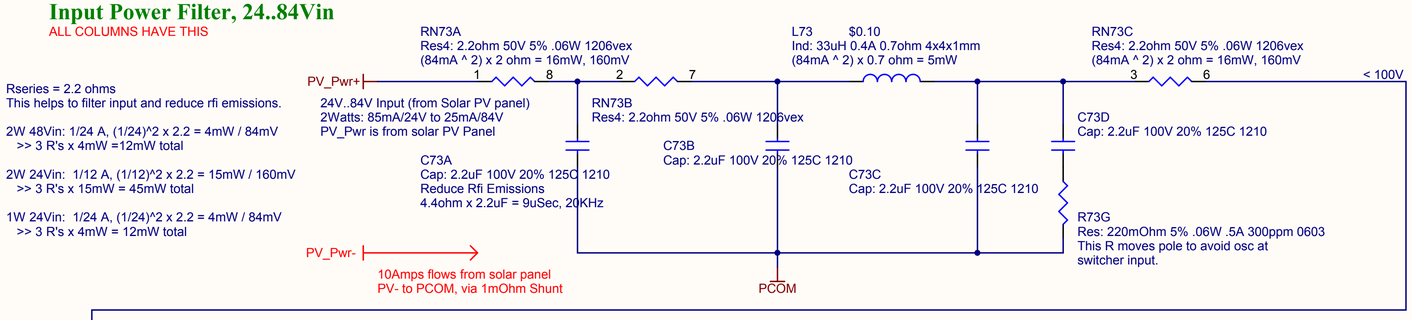
24..84V in to 10V/0.2A/2W out DC-to-DC Converter,
Non-Isolated, Regulated

DESIGN FILES

> Simulation: 24..84Vin-to-10Vout_2W_200mA_LM5163_Tina_v5a.TSC
> Analysis: GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "DESIGN: 24..84V in to 10V/2A/2W out..", "and Voltage Range Strategy...", and "300W Component Characteristics As Noted in Datasheets"
> TI Reports: "24..84Vin-to-10Vout_2W_200mA_LM5163_QuickstartCalculator.xlsm" and "24..84Vin-to-10Vout_2W_200mA_LM5163_WebBenchReport.pdf"

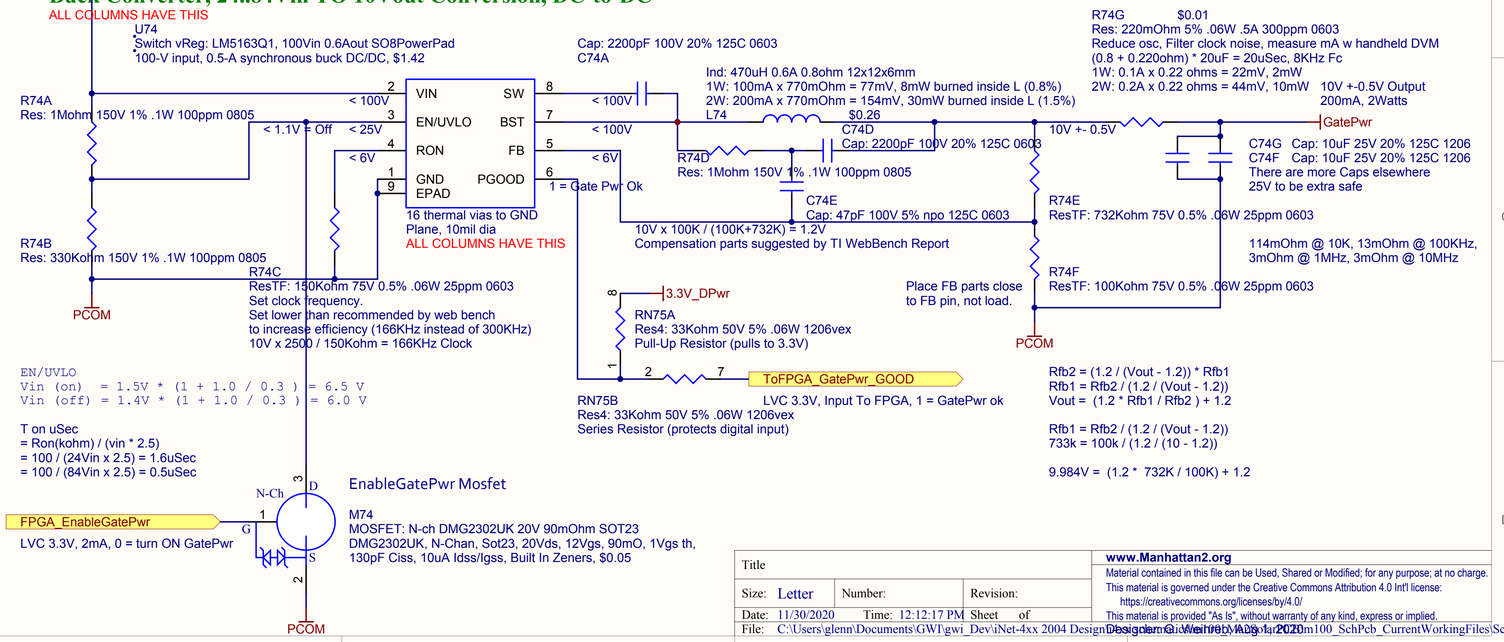
Input Power Filter, 24..84Vin

ALL COLUMNS HAVE THIS



Buck Converter, 24..84Vin TO 10Vout Conversion, DC-to-DC

ALL COLUMNS HAVE THIS



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File: C:\Users\glenn\Documents\GWI\gwi_Dev\iNet-4xx 2004 Designs\Designs Gwi\m100_Jan2020\m100_SchPcb_CurrentWorkingFiles\Schematics\m100 Specific\m100_24to84V_TO_10V_2W_PowerSupply.SchDoc			

Create 3.3Vreference (buffered and unbuffered versions)

COLUMN #1 ONLY

SUMMARY

> Convert 4.3V (Analog Pwr) to 3.3Vreference
> Buffer 3.3Vreference (drives dynanic loads such as a/d vRef input pin)

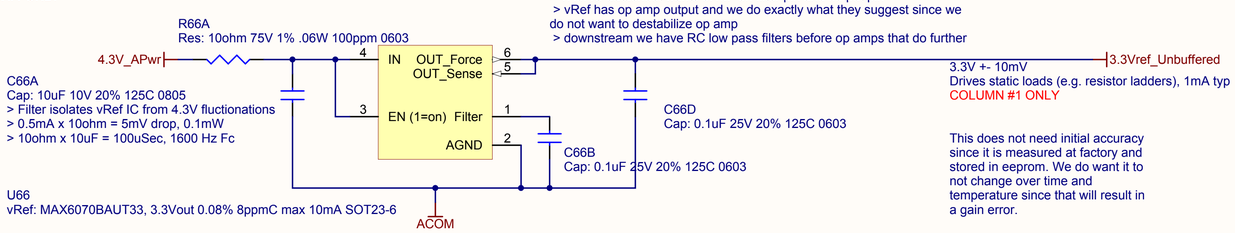
DESIGN FILES

> Simulation: "3.3Vref_OpAmpBuffer...TSC" and "vCalibration_Circuit...TSC"
> Analysis: GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "Calibration System", "vRef IC Accuracy", "Power Voltage Range Strategy...", "Component Characteristics As Noted in Datasheets"
> Ma2_Solar_RD_PLAN.pdf / "Power Supply and Voltage Reference"

Create 3.3Vreference (unbuffered)

COLUMN #1 ONLY

> vRef IC datasheet wants 0.1uF on filter pin and output pin
> vRef has op amp output and we do exactly what they suggest since we do not want to destabilize op amp
> downstream we have RC low pass filters before op amps that do further



3.3V +- 10mV
Drives static loads (e.g. resistor ladders), 1mA typ
COLUMN #1 ONLY

This does not need initial accuracy since it is measured at factory and stored in eeprom. We do want it to not change over time and temperature since that will result in a gain error.

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DC-to-DC Converter, +3.3V Input (3.3V_DPwr), -1V/30mA/30mW Output (-1V_APwr)

COLUMN #1 ONLY We need to make larger to support more columns.

SUMMARY

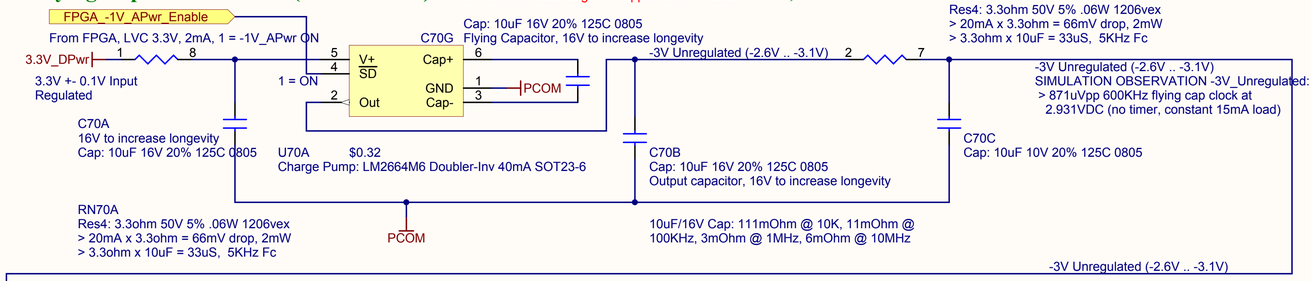
> 3.3V +- 0.1 Input TO 1V +- 0.05V (30mA/30mW) Output, DC-to-DC Converter, Non-Isolated, Regulated
> 15mA x 2V drop = 30mW wasted power, 33% efficient.
> Accuracy: +-85mV = 8.5% x 1V = 1% (Op Amp 10mVos, 0.01V/1V = 1%) + 2% (1% + 1% shunt resistors) + 1% (TLV431 shunt) + 4.5% (0.3O x 15mA = 45mV, 45mV/1V = 4.5%)
> Cost: $0.74 = 0.32 + (3 * 0.035) + (0.025) + (0.01 * 2) + 0.08 + 0.13 + 0.03 + 0.024

DESIGN FILES

```
> Simulation: 3.3Vpwr_to_-1Vpwr_Conversion_QuickSim_SIMPLE_CAPS_Pnp_v2a
 > Analysis:   GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "DESIGN: +3.3Vin to -1VDC...", "Power and Voltage Range Strategy...", and "300W Component Characteristics As No in Datasheets"
```

Flying Capacitor Inverter (+3.3V to -3V)

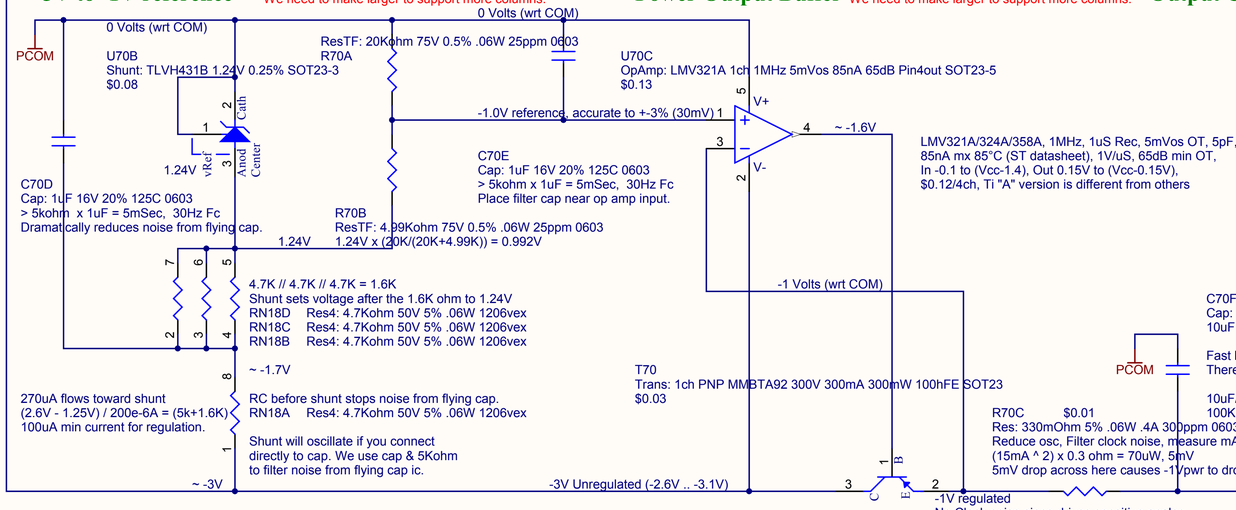
COLUMN #1 ONLY
We need to make larger to support more columns.



Filter, 5KHz

-3V to -1V reference

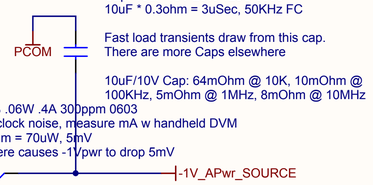
COLUMN #1 ONLY
We need to make larger to support more columns.



Power Output Buffer

COLUMN #1 ONLY
We need to make larger to support more columns.

Output Capacitor



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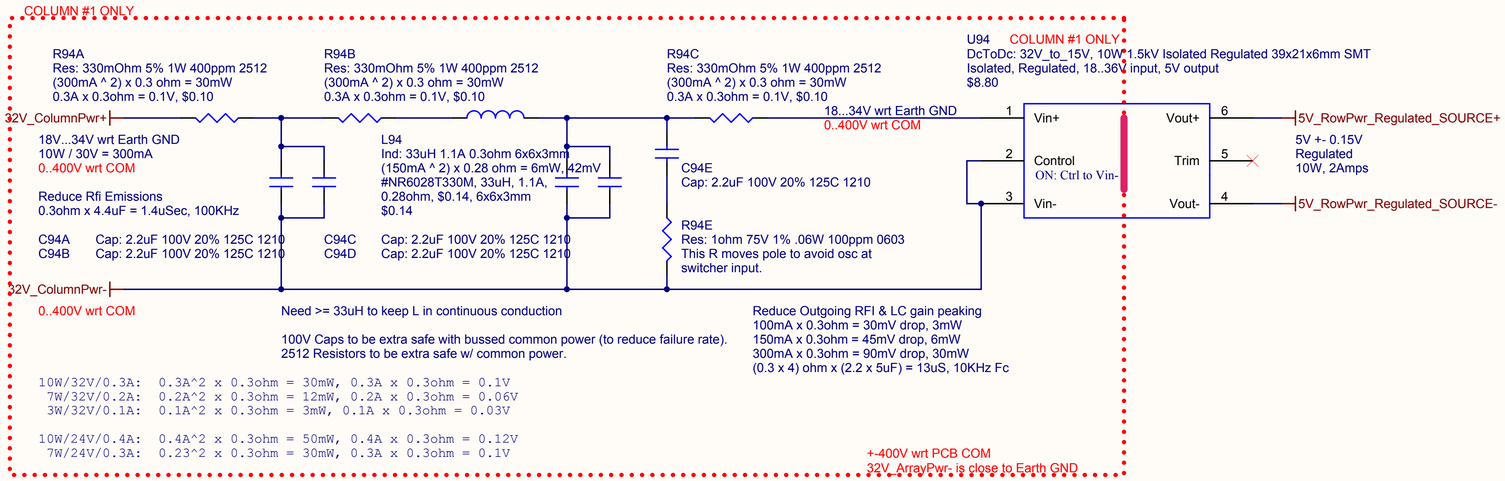
Power Filter At Input of Isolated 18..36VDC-to-5VDC Converter, 10Watt

Reduces RFI emissions, reduces current/voltage fluctuation on bussed 32V Array Power
COLUMN #1 ONLY

Isolated 18..36VDC-to-5VDC 10Watt Converter



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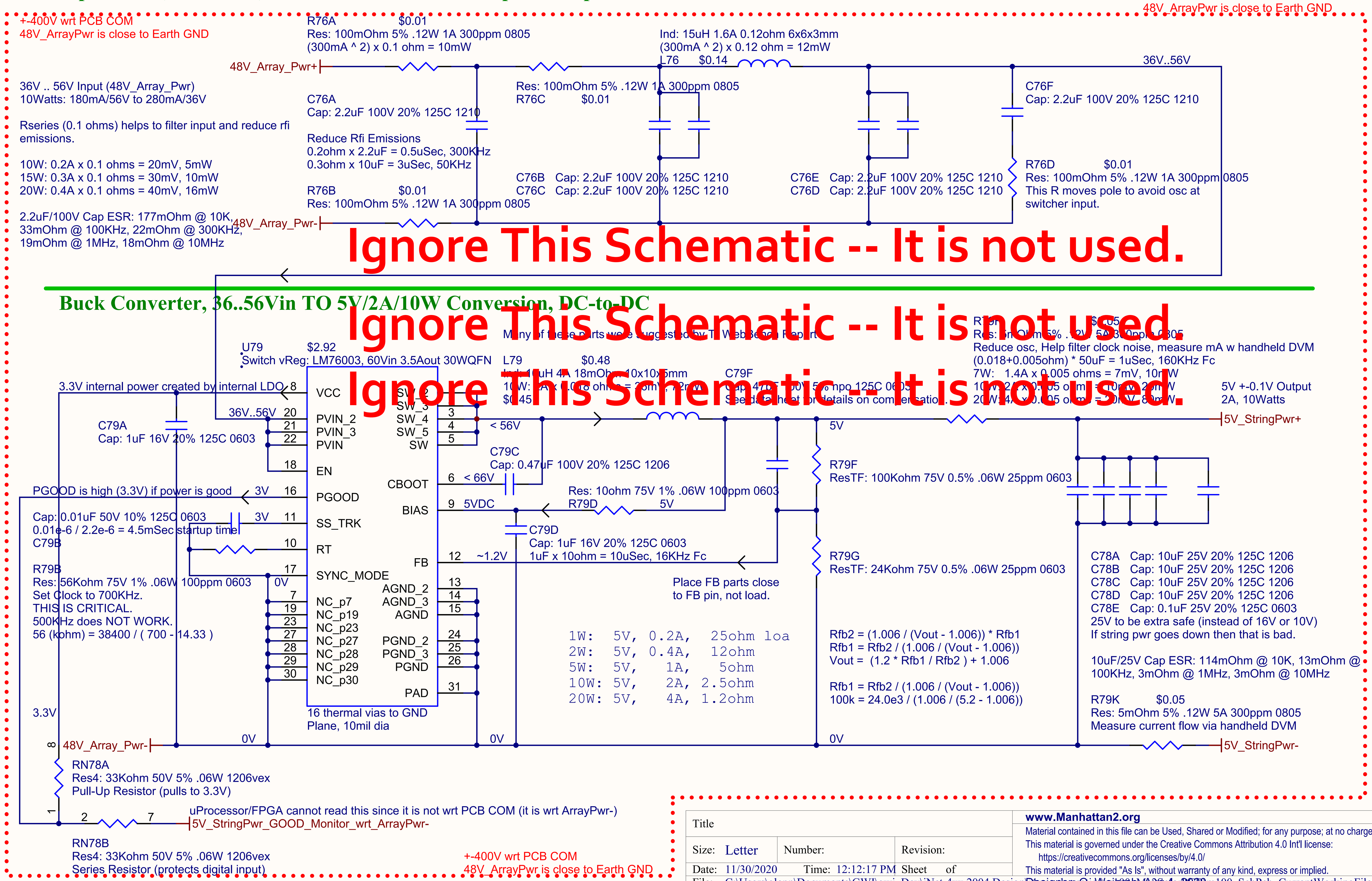
DC-to-DC Converter, 48V Input, 5V/2A/10W Output

Convert 48V-Array-Power TO 5V-String-Power

SUMMARY
> 48V (36..56V) Input TO 5V/2A/10W Output DC-to-DC Converter, Non-Isolated, Regulated
> Convert "48V-Array-Pwr" to "5V-String-Pwr"

DESIGN FILES
> Simulation: 48Vin-to-5Vout_10W_2A_LM76003_v9a.TSC
> Analysis: GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "DESIGN: 36..56V in to 5V/2A/10W..", "Power and Voltage Range Strategy...", and "300W Component Characteristics As Noted in Datasheets"
> TI Reports: "48Vin-to-5Vout_10W_2A_LM76003_SIMULATION_RESULTS_&_DESIGN_NOTES.xlsx" and "48Vin-to-5Vout_10W_2A_LM76003_TiWebBenchReport.pdf"
> Ma2_Solar_RD_PLAN.pdf / "48V-Array-Power and 5V-String-Power" and "Array of 300W Converters"

Input Filter, 36..56Vin, reduces radiated RFI and provides power to converter.



+-400V wrt PCB COM
48V_ArrayPwr is close to Earth GND
R76A $0.01
Res: 100mOhm 5% .12W 1A 300ppm 0805
(300mA ^ 2) x 0.1 ohm = 10mW
Ind: 15uH 1.6A 0.12ohm 6x6x3mm
(300mA ^ 2) x 0.12 ohm = 12mW
L76 $0.14
48V_Array_Pwr+
36V..56V
36V .. 56V Input (48V_Array_Pwr)
10Watts: 180mA/56V to 280mA/36V
Rseries (0.1 ohms) helps to filter input and reduce rfi emissions.
10W: 0.2A x 0.1 ohms = 20mV, 5mW
15W: 0.3A x 0.1 ohms = 30mV, 10mW
20W: 0.4A x 0.1 ohms = 40mV, 16mW
2.2uF/100V Cap ESR: 177mOhm @ 10K, 33mOhm @ 100KHz, 22mOhm @ 300KHz, 19mOhm @ 1MHz, 18mOhm @ 10MHz
C76A
Cap: 2.2uF 100V 20% 125C 1210
Reduce Rfi Emissions
0.2ohm x 2.2uF = 0.5uSec, 300KHz
0.3ohm x 10uF = 3uSec, 50KHz
Res: 100mOhm 5% .12W 1A 300ppm 0805
R76C $0.01
C76F
Cap: 2.2uF 100V 20% 125C 1210
C76B Cap: 2.2uF 100V 20% 125C 1210
C76C Cap: 2.2uF 100V 20% 125C 1210
C76E Cap: 2.2uF 100V 20% 125C 1210
C76D Cap: 2.2uF 100V 20% 125C 1210
R76D $0.01
Res: 100mOhm 5% .12W 1A 300ppm 0805
This R moves pole to avoid osc at switcher input.
R76B $0.01
Res: 100mOhm 5% .12W 1A 300ppm 0805
48V_Array_Pwr-
Ignore This Schematic -- It is not used.
Buck Converter, 36..56Vin TO 5V/2A/10W Conversion, DC-to-DC
Ignore This Schematic -- It is not used.
Ignore This Schematic -- It is not used.
Many of these parts were suggested by TI WebBench Report.
U79 $2.92
Switch vReg: LM76003, 60Vin 3.5Aout 30WQFN
L79 $0.48
C79F
Reduce osc, Help filter clock noise, measure mA w handheld DVM
(0.018+0.005ohm) * 50uF = 1uSec, 160KHz Fc
7W: 1.4A x 0.005 ohms = 7mV, 10mW
5V +-0.1V Output
2A, 10Watts
3.3V internal power created by internal LDO
VCC
SW_1
SW_3
SW_4
SW_5
SW
PVIN_2
PVIN_3
PVIN
EN
PGOOD
SS_TRK
RT
SYNC_MODE
NC_p7
NC_p19
NC_p23
NC_p27
NC_p28
NC_p29
NC_p30
CBOOT
BIAS
FB
AGND_2
AGND_3
AGND
PGND_2
PGND_3
PGND
PAD
36V..56V
< 56V
< 66V
5VDC
~1.2V
5V
5V_StringPwr+
C79A
Cap: 1uF 16V 20% 125C 0603
C79C
Cap: 0.47uF 100V 20% 125C 1206
R79F
ResTF: 100Kohm 75V 0.5% .06W 25ppm 0603
PGOOD is high (3.3V) if power is good
3V
Cap: 0.01uF 50V 10% 125C 0603
0.01e-6 / 2.2e-6 = 4.5mSec startup time
C79B
Res: 10ohm 75V 1% .06W 100ppm 0603
R79D
C79D
Cap: 1uF 16V 20% 125C 0603
1uF x 10ohm = 10uSec, 16KHz Fc
R79G
ResTF: 24Kohm 75V 0.5% .06W 25ppm 0603
R79B
Res: 56Kohm 75V 1% .06W 100ppm 0603
Set Clock to 700KHz.
THIS IS CRITICAL.
500KHz does NOT WORK.
56 (kohm) = 38400 / (700 - 14.33)
0V
Place FB parts close to FB pin, not load.
1W: 5V, 0.2A, 25ohm load
2W: 5V, 0.4A, 12ohm
5W: 5V, 1A, 5ohm
10W: 5V, 2A, 2.5ohm
20W: 5V, 4A, 1.2ohm
Rfb2 = (1.006 / (Vout - 1.006)) * Rfb1
Rfb1 = Rfb2 / (1.006 / (Vout - 1.006))
Vout = (1.2 * Rfb1 / Rfb2) + 1.006
Rfb1 = Rfb2 / (1.006 / (Vout - 1.006))
100k = 24.0e3 / (1.006 / (5.2 - 1.006))
C78A Cap: 10uF 25V 20% 125C 1206
C78B Cap: 10uF 25V 20% 125C 1206
C78C Cap: 10uF 25V 20% 125C 1206
C78D Cap: 10uF 25V 20% 125C 1206
C78E Cap: 0.1uF 25V 20% 125C 0603
25V to be extra safe (instead of 16V or 10V)
If string pwr goes down then that is bad.
10uF/25V Cap ESR: 114mOhm @ 10K, 13mOhm @ 100KHz, 3mOhm @ 1MHz, 3mOhm @ 10MHz
3.3V
16 thermal vias to GND Plane, 10mil dia
48V_Array_Pwr-
R79K $0.05
Res: 5mOhm 5% .12W 5A 300ppm 0805
Measure current flow via handheld DVM
5V_StringPwr-
RN78A
Res4: 33Kohm 50V 5% .06W 1206vex
Pull-Up Resistor (pulls to 3.3V)
uProcessor/FPGA cannot read this since it is not wrt PCB COM (it is wrt ArrayPwr-)
5V_StringPwr_GOOD_Monitor_wrt_ArrayPwr-
RN78B
Res4: 33Kohm 50V 5% .06W 1206vex
Series Resistor (protects digital input)
+-400V wrt PCB COM
48V_ArrayPwr is close to Earth GND

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Designer: Glenn Weinreb, Aug 1, 2020

www.Manhattan2.org

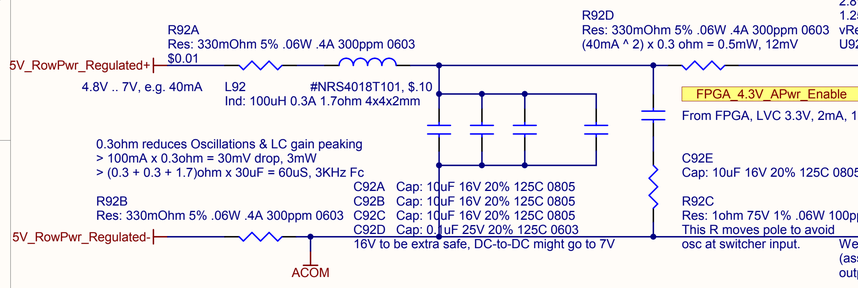
Filter Between DC-to-DC Converter Output, and Analog Power

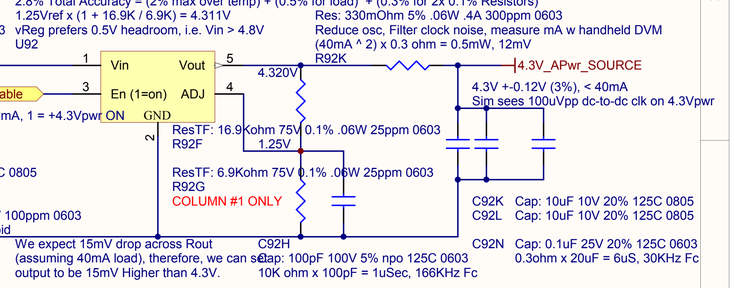
COLUMN #1 ONLY

We need to make power supplies larger to support more columns.

Reduce noise from DC-to-DC converter that enters Analog Power

Observed on Sim: Converts 20KHz 200mVpp square wave from Dc-to-Dc output into a 5mVpp sinewave and takes out higher frequencies.





Generate 3.6V Analog Power with linear vReg IC

COLUMN #1 ONLY

We need to make power supplies larger to support more columns.

DESIGN FILES

```
> Simulation: 5Vpwr_to_smaller_Vpwr_SlowSim_PRECISE_CAPS_...TSC
 > Analysis:   GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "DESIGN: 5Vin to
4.3V/3.6V...", "Power and Voltage Range Strategy...", and "300W Component Characteristics A
Noted in Datasheets"
```


3.45V_Clamp (current sink)

COLUMN #1 ONLY

We need to make larger to support more columns.

DESIGN FILES

```
> Simulation: "3.45V_Clamp_Via_Shunt...TSC"
 > Analysis:   GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "Analog Clamping
Protects A/D IC Input from over-current"
```


Title			**www.Manhattan2.org**
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Designer: G. Weinreb, Aug 1, 2020

DC-to-DC Converter, 5V/100mA Input, 3.3V/150mA Output (500mW, 3.3V Digital Power)

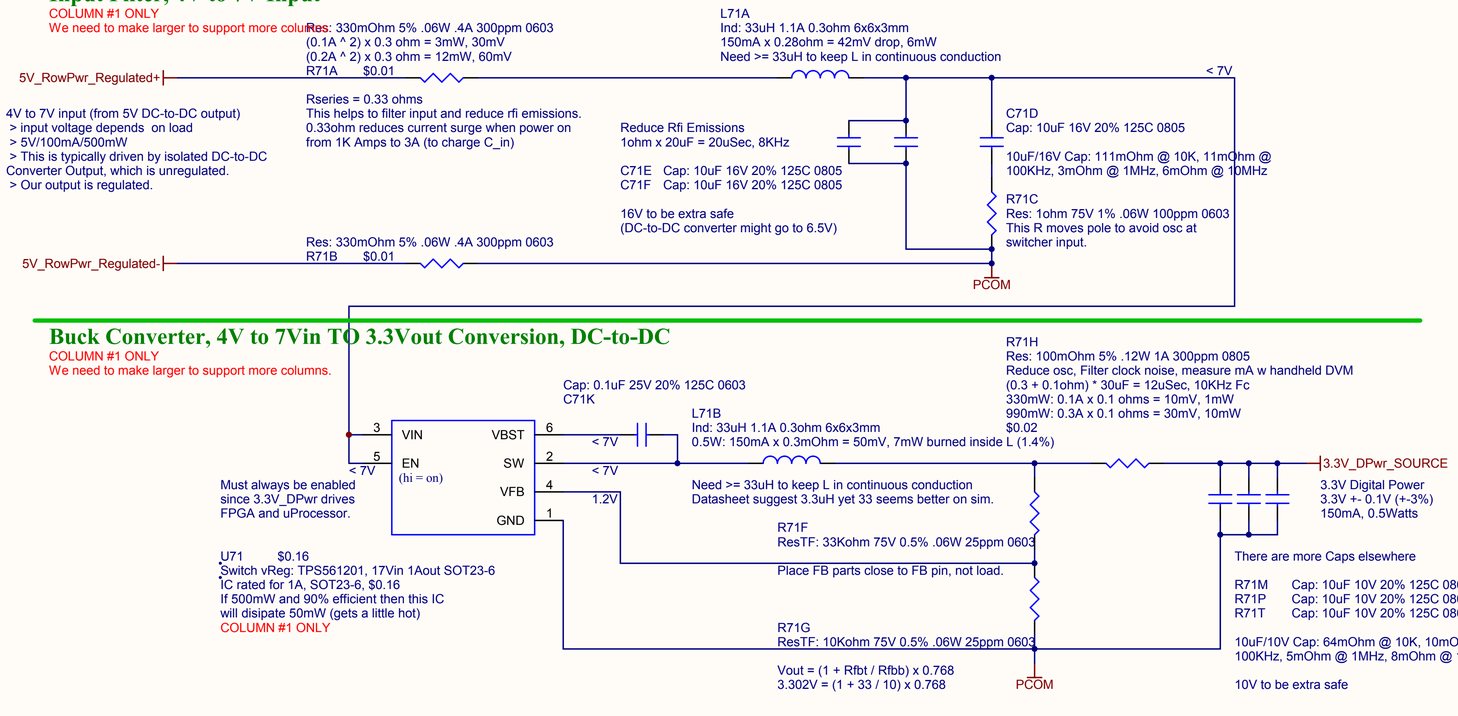
COLUMN #1 ONLY
We need to make larger to support more columns.

SUMMARY
4V to 7V Input TO 3.3V +- 0.1V (0.15A/500mW) Output DC-to-DC Converter, Non-Isolated, Regulated
$0.68 = (.035*3) + (.14) + (.16) + (.14) + (.01*2) + (.02*6)

DESIGN FILES
> Simulation: TPS561201_5V_to_3.3V_17Vin_SlowSim_PRECISE_CAPS_v3a.TSC.TSC
> Analysis: GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "DESIGN: 5V in to 3.3V/130mA/500mW...", "Power and Voltage Range Strategy...", and "300W Component Characteristics As in Datasheets"

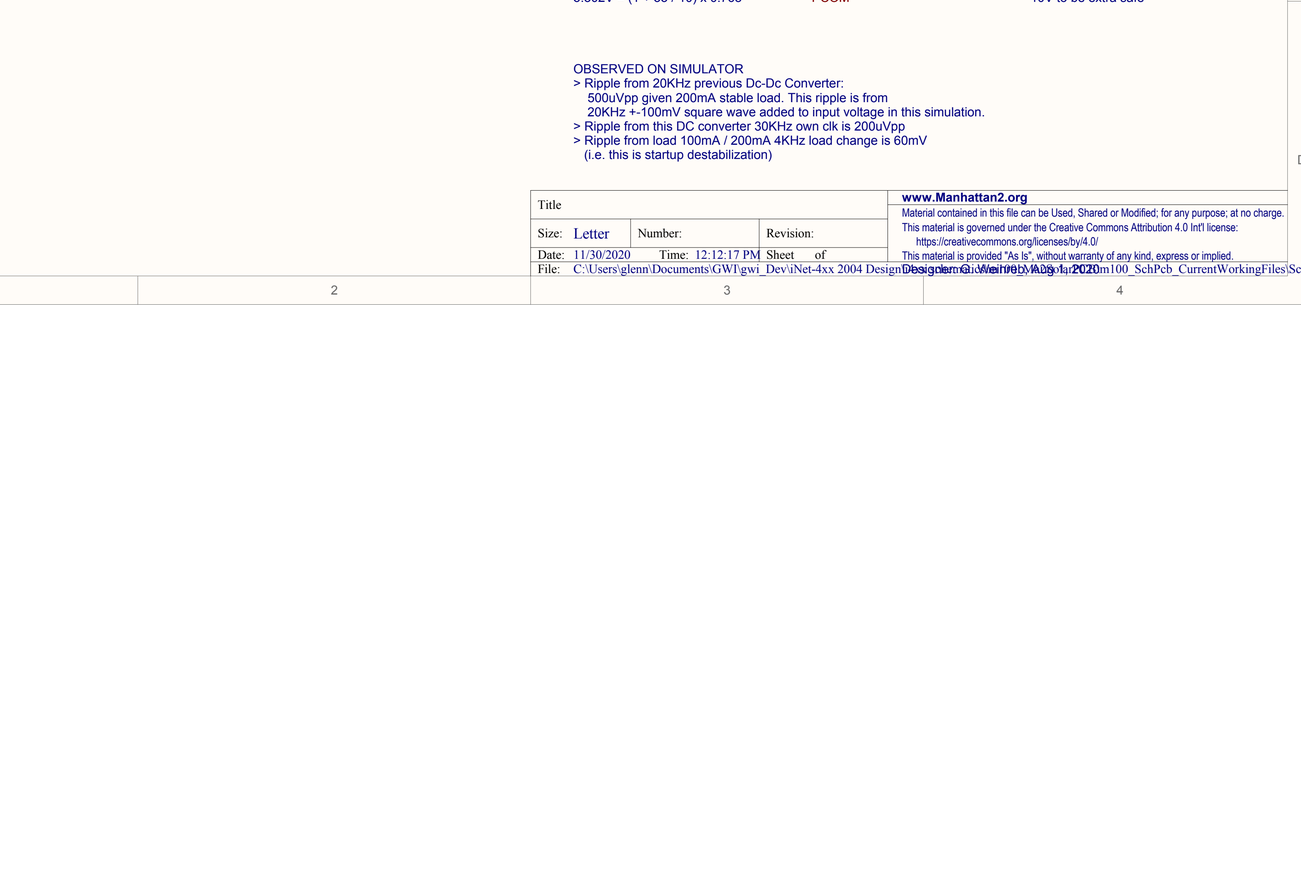
Input Filter, 4V to 7V Input

COLUMN #1 ONLY
We need to make larger to support more columns.



Buck Converter, 4V to 7Vin TO 3.3Vout Conversion, DC-to-DC

COLUMN #1 ONLY
We need to make larger to support more columns.



OBSERVED ON SIMULATOR
> Ripple from 20KHz previous Dc-Dc Converter:
500uVpp given 200mA stable load. This ripple is from
20KHz +-100mV square wave added to input voltage in this simulation.
> Ripple from this DC converter 30KHz own clk is 200uVpp
> Ripple from load 100mA / 200mA 4KHz load change is 60mV
(i.e. this is startup destabilization)

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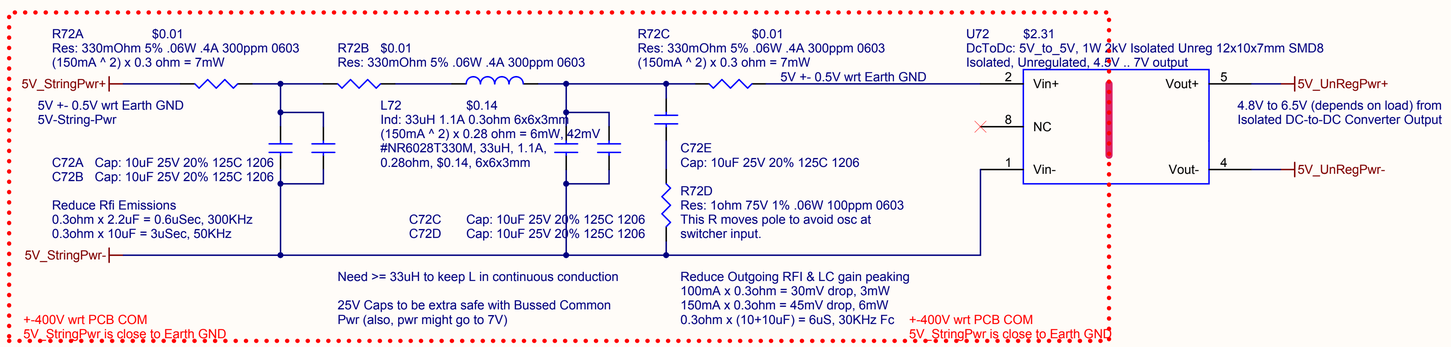
Power Filter At Input of Isolated 5VDC-to-5VDC Converter

Reduces RFI emissions, reduces current/voltage fluctuation on bussed 5Vpwr.

Isolated 5VDC-to-5VDC Converter



Ignore This Schematic -- It is not used.

Ignore This Schematic -- It is not used.
Ignore This Schematic -- It is not used.

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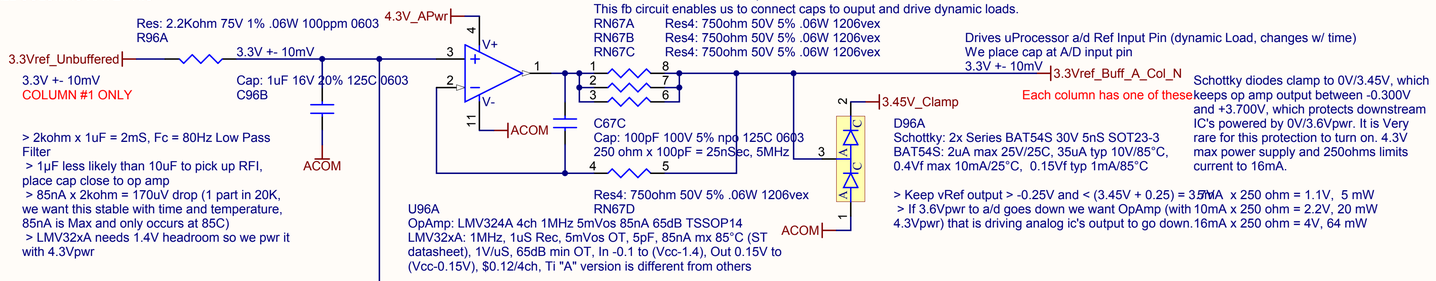
3.3V Buffered, for uProcessor ref input

ALL COLUMNS HAVE THIS



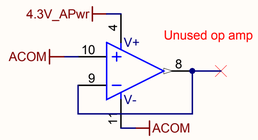
3.3V Buffered, for 16bit a/d ref input

Similar to above circuit

ALL COLUMNS HAVE THIS

2.81V Buffered, offset for main amplifier

Unused Op Amp



OpAmp: LMV324A 4ch 1MHz 5mVos 85nA 65dB TSSOP14
U96D

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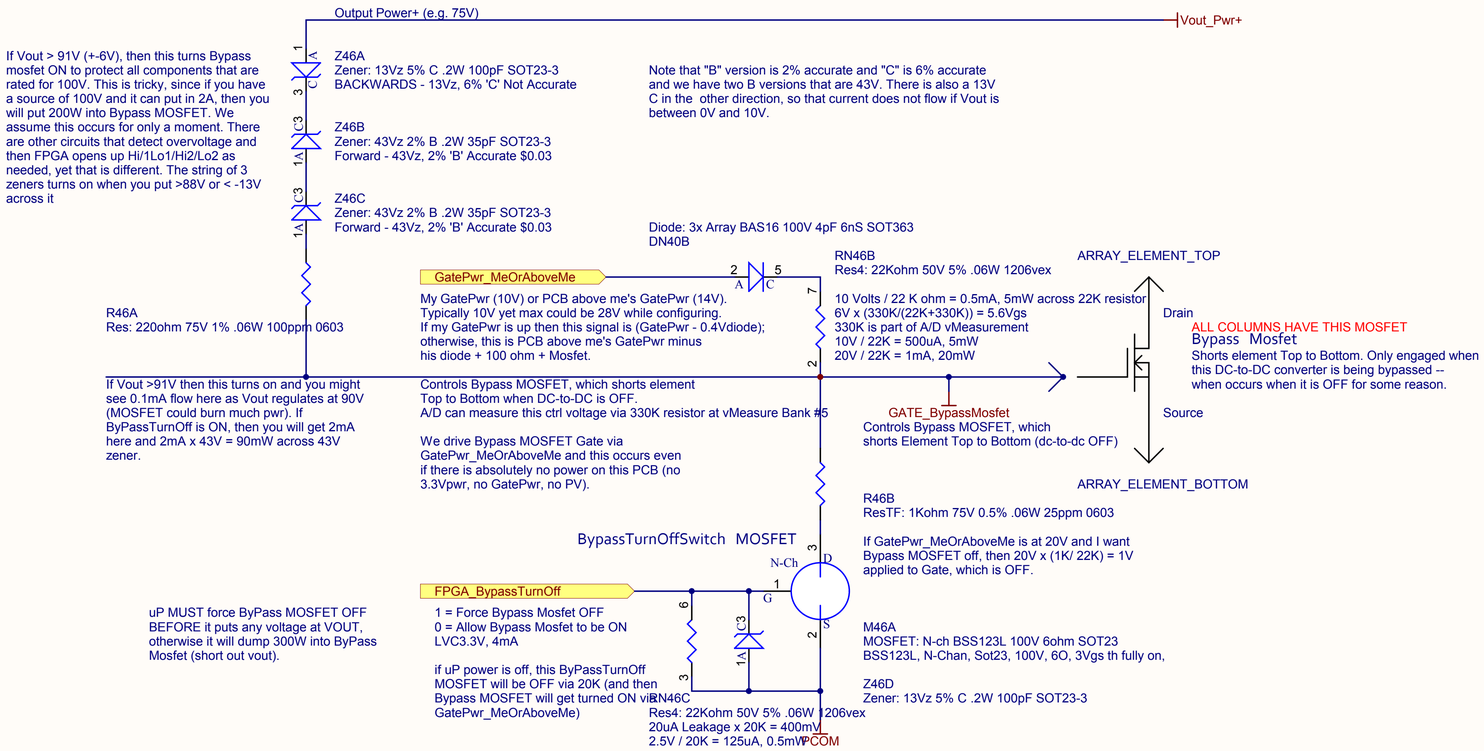
Bypass Mosfet Control Circuit

COLUMN #1 ONLY

DESIGN FILES

> Simulation: "ByPass_Mosfet_v3a.TSC"
> Analysis: GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "GatePwr (10V) AboveMe Circ



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Generate Master Calibration Voltage (switchable)

SUMMARY

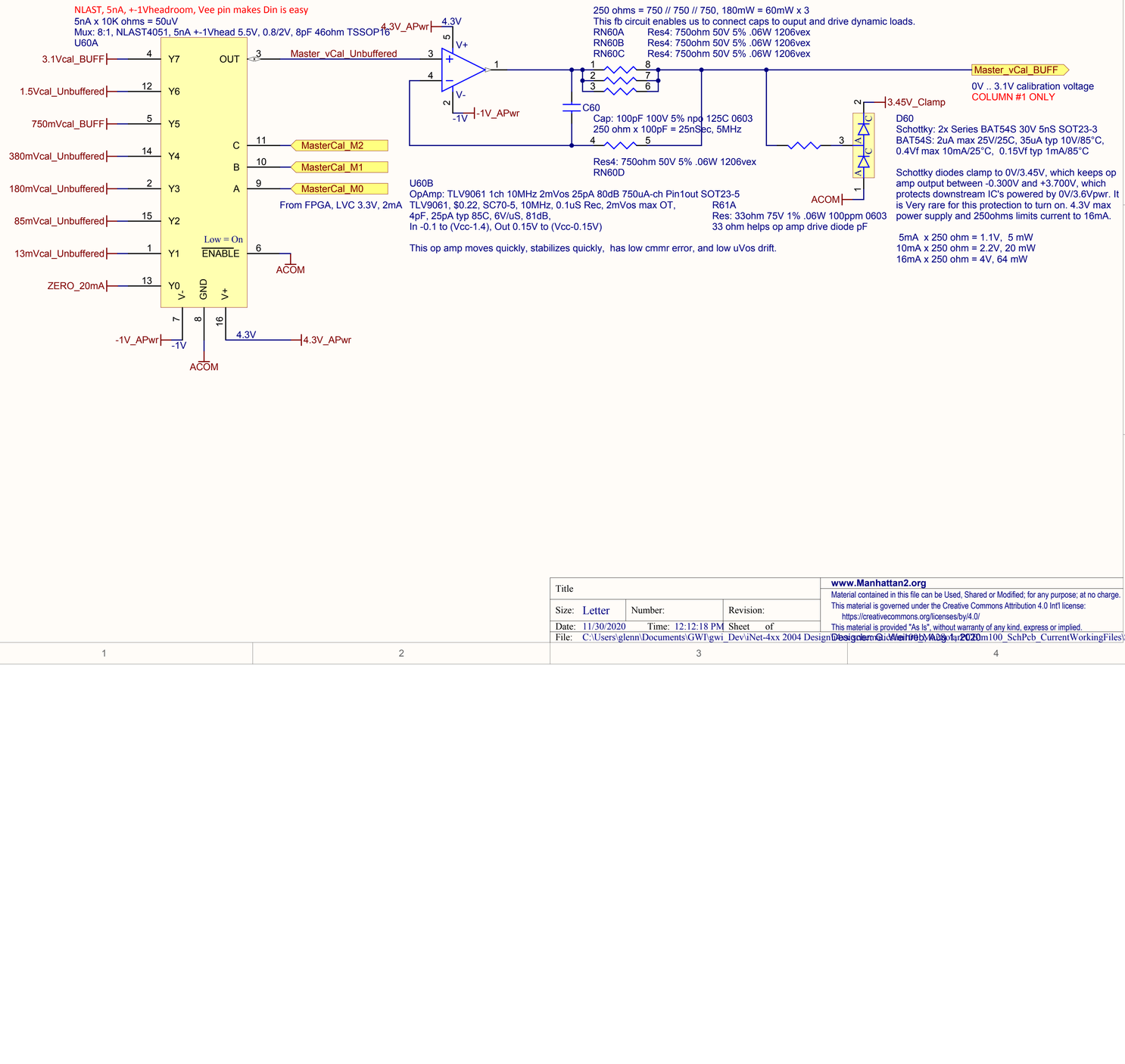
> create master calibration voltage which is switchable
> these do not need to be accurate since 16bit a/d measures them when we power up calibration. we want them to be stable After power up cal.

DESIGN FILES

> Simulation: "vCalibration_Circuit...TSC"
> Analysis: GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "Calibration System", "vRef IC Accuracy", "Power Voltage Range Strategy...", "Component Characteristics As Noted in Datasheets"
> Ma2_Solar_RD_PLAN.pdf / "Power Supply and Voltage Reference"

Select Master Calibration Voltage

Calculations: GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "Calibration System"
COLUMN #1 ONLY



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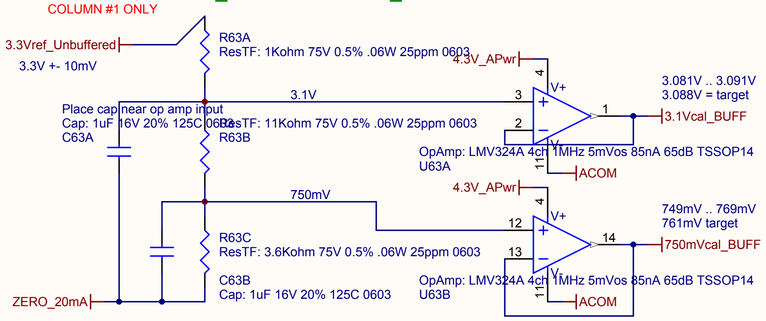
Create 3.3Vref, Buffer 3.3Vref, Create Calibration Voltages

SUMMARY
> create calibration voltages
> these do not need to be accurate since 16bit a/d measures them when we power up calibration. we want them to be stable After power up cal.

DESIGN FILES
> Simulation: "vCalibration_Circuit...TSC"
> Analysis: GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "Calibration System", "vRef IC Accuracy", "Power Voltage Range Strategy...", "Component Characteristics As Noted in Datasheets"
> Ma2_Solar_RD_PLAN.pdf / "Power Supply and Voltage Reference"

Generate 3.1Vcal_Buf & 750mVcal_Buf

COLUMN #1 ONLY



> 1K ohm x 1uF = 1mS, Fc = 160Hz
> 11K ohm x 1uF = 11mS, Fc = 16Hz
> 1uF less likely than 10uF to pick up RFI
> place cap close to op amp
> 85nA leakage from op amp does not effect vout since it spreads evenly into resistor ladder
> LMV32x needs 1.4V headroom so we pwr it with 4.3Vpwr

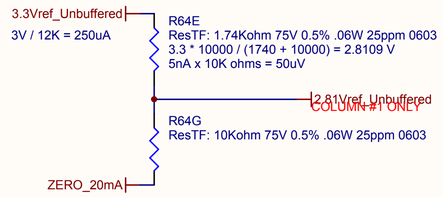
LMV32xA: 1MHz, 1uS Rec, 5mVos OT, 5pF, 85nA mx 85°C (ST datasheet), 1V/uS, 65dB min OT, In -0.1 to (Vcc-1.4), Out 0.15V to (Vcc-0.15V), $0.12/4ch, Ti "A" version is different from others

Generate Unbuffered Ref Voltages (94mV, 220mV)

Calculations: GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "Calibration System"
COLUMN #1 ONLY

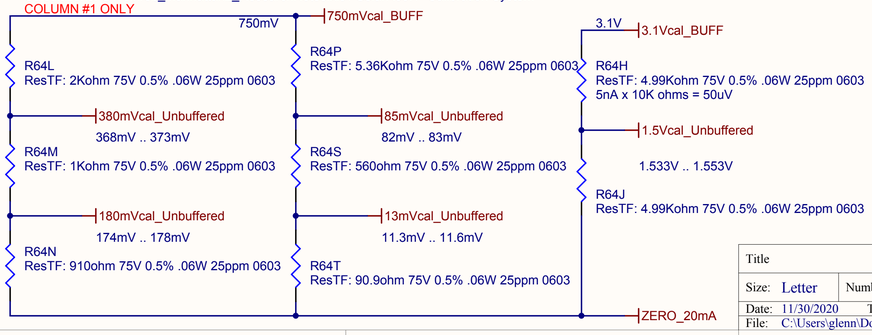
Generate Buffered Ref Voltages (2.81V)

Calculations: GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "Calibration System"
COLUMN #1 ONLY



Generate Unbuffered Calibration Voltages (13mV, 85mV, 180mV, 380mV, 1.5V)

Calculations: GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "Calibration System"
COLUMN #1 ONLY



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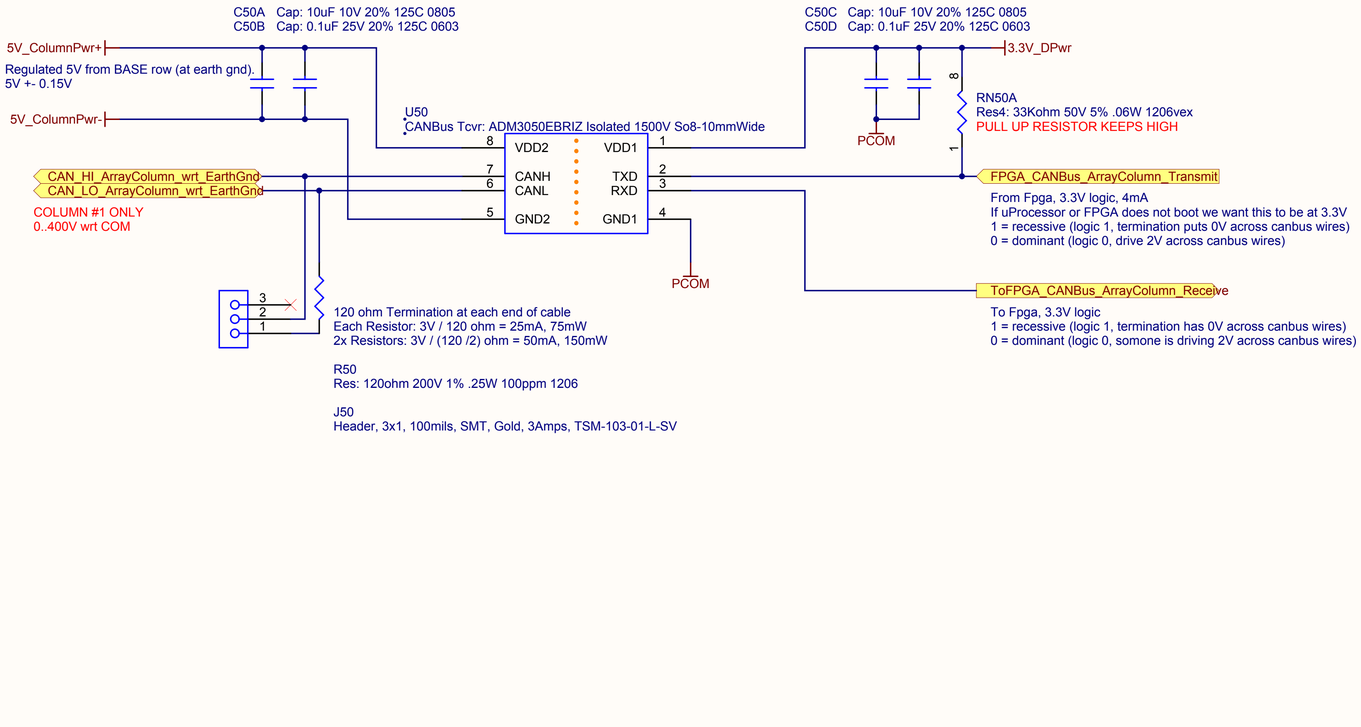
ISOLATED CANbus Transciever, Connect Elements in 1st Array Column

COLUMN #1 ONLY



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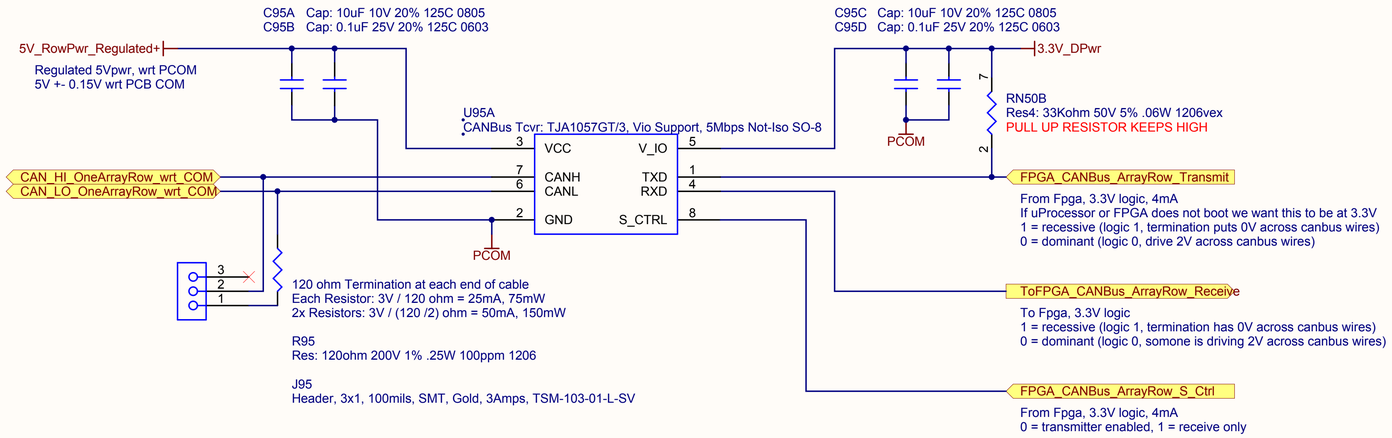
NON-ISOLATED CANbus Transciever, Connects elements within one horizontal row

ALL COLUMNS HAVE THIS



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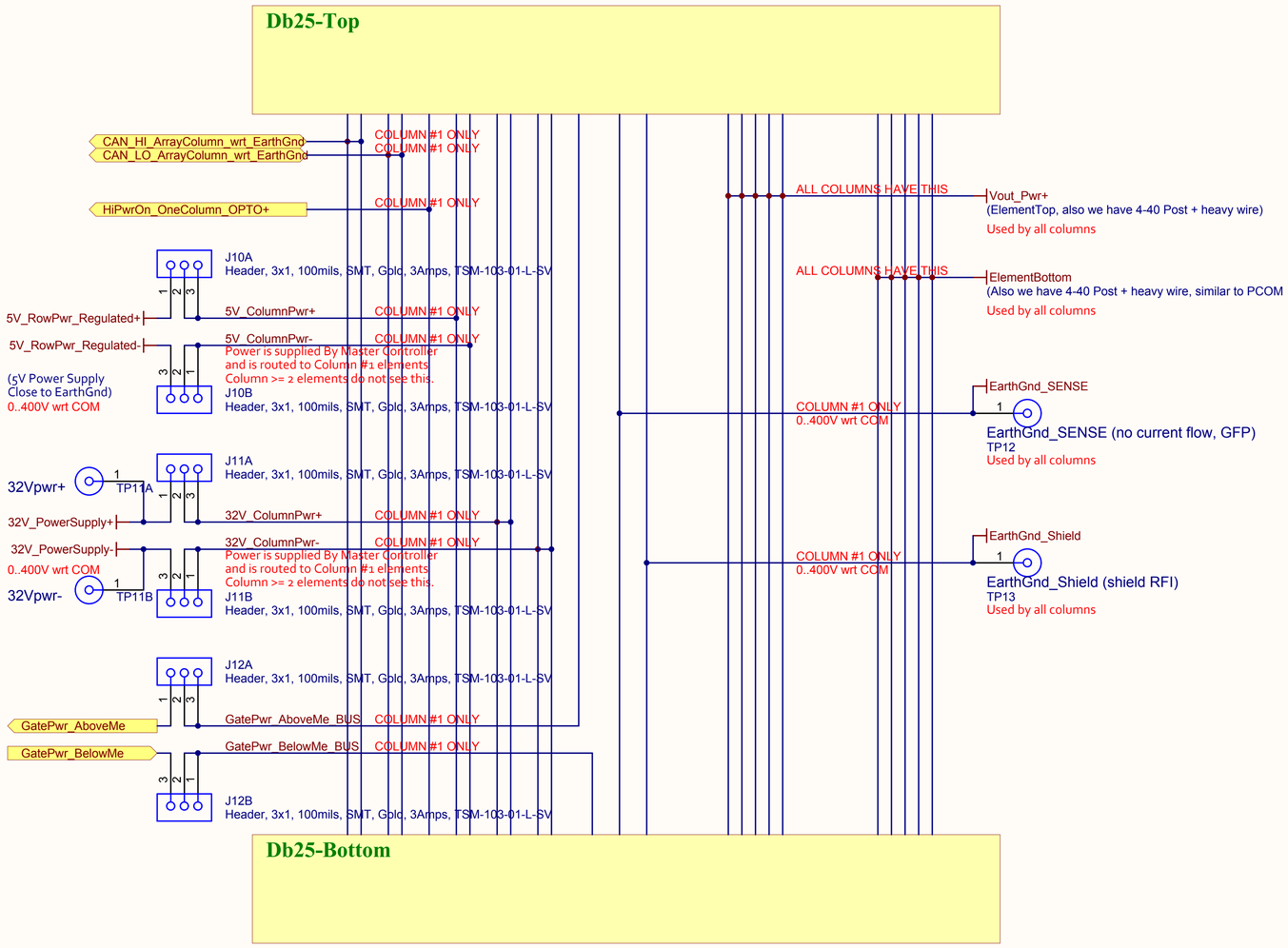
Column Connectors -- Connect together Multiple PCB's Between Rows (i.e. on a column)



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Current Measurement (via 1m ohm shunts)

For simulation, see "CurrentShunt_DiffAmp, v1za.TSC"
For analysis, see GWeinreb_Manhattanz_ResearchNotes.xls / SolarRoof / "DESIGN: DIFFERENTIAL AMPLFIER Measures ~4 to 15mV across Rshunt..."
ALL COLUMNS HAVE THIS

ALL COLUMNS HAVE THIS
50nA, pin 7 n/c, pin 10 = A, 19%/25% Din, Drive w 10k // 10K divider & -1Vpwr, $0.15
50nA x 500 ohms = 25uV
Mux: 2x 4:1, TMUX1309, 45nA +-1Vhead 5.5V, 19%/25%, 11pF 220ohm TSSOP16
U80

vMeas_Shunt1_InputPwr+
vMeas_Shunt1_InputPwr-
vMeas_Shunt2_PvPwr+
vMeas_Shunt2_PvPwr-
vMeas_Shunt3_Buck+
vMeas_Shunt3_Buck-
vMeas_Shunt4_Boost+
vMeas_Shunt4_Boost-

1A OUTA, 1B OUTB, 2A, 2B, 3A, 3B, 4A, 4B ENABLE, Low = On, Pin10 = A, N/C, GNDp, V+

-1V_APwr, -1V, 4.3V, 4.3V_APwr

Provide +-1V headroom via -1V/4.3Vpwr
19% / 25% digital inputs receive:
Logic 1: 1.96V wrt pin8 > [25% x (4.3V - -1V) = 1.38V]
Logic 0: 0.66V wrt pin8 < [19% x (4.3V - -1V) = 1.05V]

IN+, IN-

RN82A Res4: 330ohm 50V 5% .06W 1206ve
RN82D Res4: 330ohm 50V 5% .06W 1206ve

RN80A Res4: 10Kohm 50V 5% .06W 1206vex
RN80B Res4: 10Kohm 50V 5% .06W 1206vex
RN80C Res4: 10Kohm 50V 5% .06W 1206vex
RN80D Res4: 10Kohm 50V 5% .06W 1206vex
RN81A Res4: 10Kohm 50V 5% .06W 1206vex
RN81B Res4: 10Kohm 50V 5% .06W 1206vex

CurrentMeas_Bank8_M1 — From FPGA, LVC 3.3V, 2mA
CurrentMeas_Bank8_M0 — From FPGA, LVC 3.3V, 2mA
CurrentMeas_Bank8_ENABLE — From FPGA, LVC 3.3V, 2mA, 0 = ON

ALL COLUMNS HAVE THIS
50nA, pin 7 n/c, pin 10 = A, 19%/25% Din, Drive w 10k // 10K divider & -1Vpwr, $0.15
Mux: 2x 4:1, TMUX1309, 45nA +-1Vhead 5.5V, 19%/25%, 11pF 220ohm TSSOP16
U81

vMeas_Shunt5_Cout+
vMeas_Shunt5_Cout-
vMeas_Shunt6_BypassMosfet+
vMeas_Shunt6_BypassMosfet-
vMeas_Shunt7_String+
vMeas_Shunt7_String-
Master_vCal_BUFF — Created by Column #1
ZERO_20mA

1A OUTA, 1B OUTB, 2A, 2B, 3A, 3B, 4A, 4B ENABLE, Low = On, Pin10 = A, N/C, GNDp, V+

-1V_APwr, -1V, 4.3V, 4.3V_APwr

Provide +-1V headroom via -1V/4.3Vpwr
19% / 25% digital inputs receive:
Logic 1: 1.96V wrt pin8 > [25% x (4.3V - -1V) = 1.38V]
Logic 0: 0.66V wrt pin8 < [19% x (4.3V - -1V) = 1.05V]

RN81C Res4: 10Kohm 50V 5% .06W 1206vex
RN81D Res4: 10Kohm 50V 5% .06W 1206vex

CurrentMeas_Bank9_ENABLE — From FPGA, LVC 3.3V, 2mA, 0 = ON

RFI Filter

S1_IN+, S1_IN-

1/(6 * (330+220) / 47e-12) = 7 MHz
Cap: 47pF 100V 5% npo 125C 0603
C82C

C82A Cap: 3pF 50V 5% npo 125C 0603
C82B Cap: 3pF 50V 5% npo 125C 0603
ACOM

Differential Amplifier (g = 2.3 x 2.4 = 5.44)

U82A
OpAmp: TLV9064 4ch 10MHz 2mVos 25pA 80dB 750uA-ch TSSOP14

R84A
ResTF: 6.9Kohm 75V 0.1% .06W 25ppm 0603
3.3V * (102 / (102+69000)) = 0.04807V
3.3Vref_Buff_B_Col_N
3.3V DC
Each column has one of these. Place R's near op amp IN+

4.3V_APwr, -1V_APwr

R83A ResTF: 102ohm 75V 0.1% .06W 25ppm 0603
g = 1 + 2 x (102 / 160) = 2.275
Low Resistors Reduces Coupling of Noise

R83B ResTF: 160ohm 75V 0.1% .06W 25ppm 0603
R83C ResTF: 102ohm 75V 0.1% .06W 25ppm 0603

S1_OUT+, S1_OUT-

R83D ResTF: 160ohm 75V 0.1% .06W 25ppm 0603
R83E ResTF: 383ohm 75V 0.1% .06W 25ppm 0603
g = 383 / 160 = 2.393
S2_IN+

R83F ResTF: 160ohm 75V 0.1% .06W 25ppm 0603
ResTF: 383ohm 75V 0.1% .06W 25ppm 0603
S2_IN-

U82C
OpAmp: TLV9064 4ch 10MHz 2mVos 25pA 80dB 750uA-ch TSSOP14

U82B
OpAmp: TLV9064 4ch 10MHz 2mVos 25pA 80dB 750uA-ch TSSOP14
TLV906x, 10MHz, 0.2uS Rec, 2mVos max OT, 4pF,
25pA typ 85C, 6VuS, 80dB min OT, In -0.1 to (Vcc-1.4), Out 0.15V to (Vcc-0.15V), 750uA/ch, $0.49

High Gain Fast Amplifier (G = 20)

R84B ResTF: 102ohm 75V 0.1% .06W 25ppm 0603
48mVcal
C84B Cap: 1uF 16V 20% 125C 0603
Place cap near op amp IN+
48mV DC

ResTF: 383ohm 75V 0.1% .06W 25ppm 0603
R84C
S2_OUT
S3_IN-

R84D ResTF: 7.68Kohm 75V 0.1% .06W 25ppm 0603
g = -7680 / 383 = -20.05, GBW = 88MHz, BW = 3MHz
C84D Cap: DNP 0603
Possibly need this to avoid gain peaking (high gain at Fc frequency)

U84
OpAmp: LMV793 1ch 88MHz 2mVos 25pA 75dB Pin1out SOT23-5
LMV794, 2Ch, $0.82, 88MHz, 1.6mVos mx OT,
25pA max OT, 28V/uS, 75dB min OT, In 0 to (Vcc-1.3V), Out 0.3V to (Vcc-0.3V)

R84E Res: 220ohm 75V 1% .06W 100ppm 0603
protect Xmc4200 from overvoltage
1V / 220 = 5mA, 5mW -- rare
4V / 220 = 18mA, 70mW -- very rare
S3_Out

Measure_7x_CurrentShunts_1.5MHz_BW
Measure current (1.5MHz BW)
Input: -5mV to +15mV (-5A to 15A w/ 1m ohm shunt)
Gain = 115, BW = 1.5MHz (obs on sim)
Output: 0 to 3.3V
ALL COLUMNS HAVE THIS

Clamp to protect uProcessor

3.45V_Clamp
R84F
Res: 33ohm 75V 1% .06W 100ppm 0603
33 ohm helps op amp drive diode pF
Protect Xmc4200 from overvoltage
D84
Schottky: 2x Series BAT54S 30V 5nS SOT23-3
BAT54S: 2uA max 25V/25C, 35uA typ 10V/85°C,
0.4Vf max 10mA/25°C, 0.15Vf typ 1mA/85°C

Low Pass Filter (Fc = 16KHz)

U82D
OpAmp: TLV9064 4ch 10MHz 2mVos 25pA 80dB 750uA-ch TSSOP14

R85A
ResTF: 10Kohm 75V 0.5% .06W 25ppm 0603
1/(6 x 10e3 x 1000e-12) = 16KHz
S4_LP_IN-
C85A
Cap: 1000pF 50V 10% 125C 0603

S4_LP_OUT
R85B
Res: 220ohm 75V 1% .06W 100ppm 0603
16KHz version of current shunt output
Protect Xmc4200 from overvoltage
Measure_7x_CurrentShunts_16KHz_BW

Vout Voltage Monitoring (3MHz BW)

For simulation, see "100Vmeasure - vDivider to Op Amp -- 300K and 7K, v1a.TSC
Calibration: measure here & also via main amp inverter to determine ratio of vDivider R's

R86A ResTF: 150Kohm 75V 0.5% .06W 25ppm 0603
R86B ResTF: 150Kohm 75V 0.5% .06W 25ppm 0603
80V / 300e3 = 250uA, 25mW
50V / 300e3 = 160uA, 8mW

Vout_Pwr+
<100V
Primary Dc-to-Dc Converter Output

R86C
ResTF: 7.68Kohm 75V 0.1% .06W 25ppm 0603
Place close to OpAmp Input
PCOM

4.3V_APwr, 4.3V, -1V, -1V_APwr

R86D
Res: 220ohm 75V 1% .06W 100ppm 0603
Protect Xmc4200 from overvoltage
C86D
Cap: 100pF 100V 5% npo 125C 0603
R86E
Res: 2.2Kohm 75V 1% .06W 100ppm 0603
C86E
Cap: 1000pF 50V 10% 125C 0603
Control Gain Peaking

U86
OpAmp: TLV9061 1ch 10MHz 2mVos 25pA 80dB 750uA-ch Pin1out SOT23-5
TLV9061, $0.22, SC70-5, 10MHz, 0.1uS Rec, 2mVos max OT,
4pF, 25pA typ 85C, 6VuS, 81dB,
In -0.1 to (Vcc-1.4), Out 0.15V to (Vcc-0.15V)

Clamp to protect uProcessor

3.45V_Clamp
R86G
Res: 33ohm 75V 1% .06W 100ppm 0603
33 ohm helps op amp drive diode pF
Protect Xmc4200 from overvoltage
D86
Schottky: 2x Series BAT54S 30V 5nS SOT23-3

Measure_Vout_5MHz_BW
Measure Output Voltage
ALL COLUMNS HAVE THIS

If you look at 300K ohm x 2pF at pin you see a 1MHz BW. Yet we are doing much more. This is due to gain peaking (according to sim) which offsets these other things. For details, see sim file ("300Vmeasure - vDivider to Op Amp -- 300K and 7K, v1a.TSC").

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Designer: G. Weinreb, Aug 1, 2020

FPGA Power Conversion

ALL COLUMNS HAVE THIS

For FPGA pin assignments, see file "FPGA_Solar_Array_Signal_Routing.xlsx"

m100_BypassMosfet_Control.SchDoc — COLUMN #1 ONLY

FPGA_BypassTurnOff → FPGA_t_1

1 = Force Bypass Mosfet OFF
0 = Allow Bypass Mosfet to be ON
LVC3.3V, 4mA

m100_GatePwr_Management.SchDoc — COLUMN #1 ONLY

FPGA_LoadDown_MeOrAboveMe → FPGA_t_2

1 = fpga loads down MeOrAboveMe via 20K ohm

FPGA_TurnOff10VaboveMe → FPGA_t_3

LVC 3.3V (logic 0 = 0.4V, logic 1 = 2.8V)
1 = Fpga turns OFF GatePwr_AboveMe
0 = Fpga turns ON GatePwr_AboveMe

m100_GateDrive_Left.SchDoc — ALL COLUMNS HAVE THIS

FPGA_GateDrive_Left_Hi → FPGA_t_4
FPGA_GateDrive_Left_Lo → FPGA_t_5

From FPGA, LVC 3.3V, 2mA
1 = turns on Left_Lo/Left_Hi mosfet

FPGA_BleedCurrent_Left → FPGA_t_6

3V: turn on 33K ohm load
FPGA programmed for 8mA output, 3.3V LVC

FPGA_GatePullDown_Left_LO → FPGA_t_7

3V: short Left_Lo gate to 0V (hold it down)
FPGA output set for 16mA with 3.3Vpwr

FPGA_GLB_Control → FPGA_t_8

3V: turns on GLB mosfet via GLBD & GLBU
and connects gate driver to Left_Lo gate
0V: turns off mosfet (isolate Left_Lo Gate from Gate Driver)

m100_GateDrive_Right.SchDoc — ALL COLUMNS HAVE THIS

FPGA_GateDrive_Right_Hi → FPGA_t_9
FPGA_GateDrive_Right_Lo → FPGA_t_10

From FPGA, LVC 3.3V, 2mA
1 = turns on Right_Lo / Right_Hi mosfet

FPGA_GatePullDown_Right_Lo → FPGA_t_11

3V: short Right_Lo gate to 0V (hold it down)
FPGA output set for 16mA with 3.3Vpwr

FPGA_BleedCurrent_Right → FPGA_t_12

3V: turn on 33K ohm load
FPGA programmed for 8mA output, 3.3V LVC

U3E

FPGA_t_1 … FPGA_t_12

FPGA_Solar_Array_Signal_Routing

m100_PowerVoltage_Monitoring.SchDoc — ALL COLUMNS HAVE THIS

ToFPGA_Overvoltage_PvPwr → FPGA_v_1

PV Power+ (solar panel out)
Open Collector Output (low if in+ > in-)
Connect to FPGA w/ internal pull-up

ToFPGA_Overvoltage_Vout_Pwr → FPGA_v_2

Primary Dc-to-Dc Converter Output
Open Collector Output (low if in+ > in-)
Connect to FPGA w/ internal pull-up

ToFPGA_Overvoltage_FiltrOut_Pwr → FPGA_v_3

Filter Output (after PV Input)
Open Collector Output (low if in+ > in-)
Connect to FPGA w/ internal pull-up

ToFPGA_Overvoltage_InductorLeft_Pwr → FPGA_v_4

Primary Inductor Input Side
Open Collector Output (low if in+ > in-)
Connect to FPGA w/ internal pull-up

ToFPGA_Overvoltage_InductorRight_Pwr → FPGA_v_5

Primary Inductor Output Side
Open Collector Output (low if in+ > in-)
Connect to FPGA w/ internal pull-up

ToFPGA_UNDERvoltage_PvPwr → FPGA_v_6

PV Power+ (solar panel out)
Open Collector Output (low if in+ > in-)
Connect to FPGA w/ internal pull-up

ToFPGA_UNDERvoltage_Vout_Pwr → FPGA_v_7

Primary Dc-to-Dc Converter Output
Open Collector Output (low if in+ > in-)
Connect to FPGA w/ internal pull-up

ToFPGA_3.6V_APwr_GOOD → FPGA_v_8

hi if analog pwr is good
Connect to FPGA w/ internal pull-DOWN

U3F

FPGA_v_1 … FPGA_v_8

FPGA_Solar_Array_Signal_Routing

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www.Manhattan2.org

Material shudown is for use to shut others to turn pwr OFF)
This material shown is only for use to shut others to turn pwr OFF (no charge.
One shutdown is only for use to others for emergency shutdown)

Designed on: Wednesday, August 26, 2020

FPGA System

ALL COLUMNS HAVE THIS

For FPGA pin assignments, see file "FPGA_Solar_Array_Signal_Routing.xlsx"

m100_Xmc_uProc_IO.SchDoc ALL COLUMNS HAVE THIS

U3C

HIB_IO_0 hibernate i/o — FPGA_w_1

RESET# uP has internal pull-up resistor, 0 = reset — FPGA_w_2

ADC_EMUX_00 Mux Channel Selection — FPGA_w_3
ADC_EMUX_01 — FPGA_w_4
ADC_EMUX_02 — FPGA_w_5
ADC_EMUX_11 — FPGA_w_6
ADC_EMUX_12 — FPGA_w_7

FPGA to uProcessor SPI Interface

SPI_FPGA_Interface_SCLK — FPGA_w_8
SPI_FPGA_Interface_MOSI — FPGA_w_9
SPI_FPGA_Interface_MISO — FPGA_w_10
SPI_FPGA_Interface_CS0 — FPGA_w_11
SPI_FPGA_Interface_CS1 — FPGA_w_12

uP_P1.2 FPGA to uProcessor DIO Interface — FPGA_w_13
uP_P1.5 — FPGA_w_14
uP_P3.0 — FPGA_w_15
uP_P0.1 — FPGA_w_16
uP_P0.3 — FPGA_w_17
uP_P0.4 — FPGA_w_18
uP_P0.5 — FPGA_w_19
uP_P0.6 — FPGA_w_20
uP_P0.8 — FPGA_w_21
uP_P0.10 — FPGA_w_22
uP_P0.11 — FPGA_w_23
uP_P2.5 — FPGA_w_24
uP_P2.6 — FPGA_w_25
uP_P2.8 — FPGA_w_26
HiHeatAlarm — FPGA_w_27

FPGA_Solar_Array_Signal_Routing

High Heat Temperature Monitor ALL COLUMNS HAVE THIS

U4
Temp Monitor: TMP302C, 90 to 105C trip OC out, SOT-563
Place in middle of DC-to-DC converter

HiHeatAlarm
0 = excess temperature, 1= ok
fpga adds pull-up, TMP302 pulls down

3 *OUT — TRIPSET0 1 — 105°C — 3.3V_DPwr
5 VS — TRIPSET1 6
2 GND — HYSTSET 4 — 5°C — ACOM

3.3V_DPwr
ACOM

fpga power, clock, spi, etc?
fpga power, clock, spi, etc?
fpga power, clock, spi, etc?

m100_Calibration_System.SchDoc COLUMN #1 ONLY

U3D

MasterCal_M2 — FPGA_p_1
MasterCal_M1 — FPGA_p_2
MasterCal_M0 — FPGA_p_3

From FPGA, LVC 3.3V, 2mA

m100_5VstringPwr_TO_LowVoltage_PowerSupply.SchDoc COLUMN #1 ONLY

FPGA_4.3V_APwr_Enable — FPGA_p_4

From FPGA, LVC 3.3V, 2mA, 1 = +4.3Vpwr ON

m100_3.3V_TO_-1V_30mA_PowerSupply.SchDoc COLUMN #1 ONLY

FPGA_-1V_APwr_Enable — FPGA_p_5

From FPGA, LVC 3.3V, 2mA, 1 = -1V_APwr ON

m100_24to84V_TO_10V_2W_PowerSupply.SchDoc ALL COLUMNS HAVE THIS

ToFPGA_GatePwr_GOOD — FPGA_p_6

LVC 3.3V, Input To FPGA, 1 = GatePwr ok

FPGA_EnableGatePwr — FPGA_p_7

LVC 3.3V, 2mA, 0 = turn ON GatePwr

m100_CANbus_NotIsolated.SchDoc ALL COLUMNS HAVE THIS

FPGA_CANBus_ArrayRow_S_Ctrl — FPGA_p_8

From Fpga, 3.3V logic, 4mA
0 = transmitter enabled, 1 = receive only

m100_Discovery_Communication.SchDoc ALL COLUMNS HAVE THIS

FPGA_Dout_ToAdjacentElement — FPGA_p_9

From FPGA, LVC 3.3V, 2mA

Recieve goes to A/D, not FPGA

m100_HiPwrOn_TmitAndRcv.SchDoc COLUMN #1 ONLY

ToFPGA_HiPwrOn_OneArrayRow_RECEIVE — FPGA_p_10

To Fpga, 3.3V logic, All Elements in One Row in Parallel
1 = HiPwrOn is not powerd (i.e. DC-to-DC is OFF)
0 = HiPwrOn has power (i.e. DC-to-DC is ON)
0 = HiPwrOn has power (i.e. DC-to-DC is ON)

FPGA_HiPwrOn_OneArrayRow_TRANSMIT — FPGA_p_11

From Fpga, 3.3V OpenCollector
All Elements in One Row in Parallel
1 = shutdown is off (we do not tell others to turn pwr OFF)
0 = shutdown is on (we tell others to do emergency shutdown)

m100_HiPwrOn_Source.SchDoc MASTER CONTROLLER O
(outside of array)

FPGA_MasterCtlr_TurnOn_HiPwrOn_SOURCE — FPGA_p_12

FPGA_Solar_Array_Signal_Routing

FPGA w/ GND pin = circuit COM From FPGA, LVC 3.3V, 2mA
MASTER CONTROLLER Only, Outside Array
1 = turn ON HiPwrOn source (set to 5V, master reset functional)
0 = turn OFF HiPwrOn source (set to 0V, master reset = ON)

Title			
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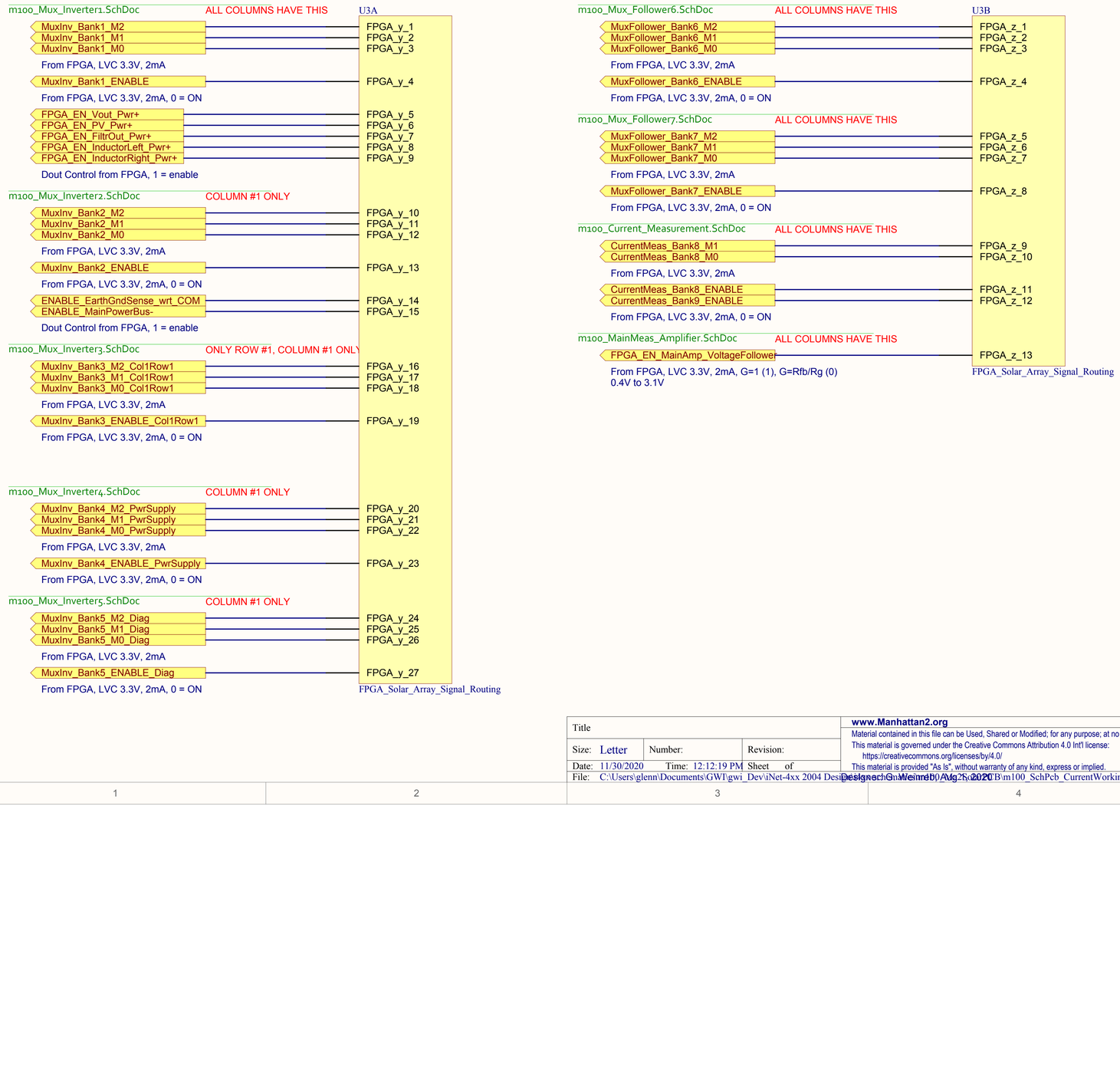
Date: 11/30/2020	Time: 12:12:19 PM	Sheet of	
File: C:\Users\glenn\Documents\GWI\gwi_Dev\iNet-4xx 2004 Designs\m100_AVG_PCB\m100_SchPcb_CurrentWorkingFiles\Schematics\m100 Specific\m100_FPGA_System.SchDoc			

Designed on Aug 27, 2020

FPGA Voltage Measurement

ALL COLUMNS HAVE THIS

For FPGA pin assignments, see file "FPGA_Solar_Array_Signal_Routing.xlsx"



Title			
Size: Letter	Number:	Revision:	
Date: 11/30/2020	Time: 12:12:19 PM	Sheet of	
File: C:\Users\glenn\Documents\GWI\gwi_Dev\iNet-4xx 2004 Design\Archive\Weinreb\Aug 25, 2020\B\m100_SchPcb_CurrentWorkingFiles\Schematics\m100 Specific\m100_FPGA_Vmeasure.SchDoc			

Gate Drive: Left of Main Inductor (i.e. drive gates of Left_Lo and Left_Hi mosfets)

For simulation, see "Gate_Drv_Testing_UCC27282_2xFet_Switch_v14f.TSC"
For simulation, see GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "Buck Converter Math"
ALL COLUMNS HAVE THIS

Input Filter
0.3 ohm x 10uF = 3 uSec, 20 KHz Fc
PEAK: 0.3A x 0.3 ohms = 100mV, 30mW
AVG: 0.2A x 0.3 ohms = 66mV, 12mW

R37A Res: 330mOhm 5% .06W .4A 300ppm 0603
C37A Cap: 10uF 25V 20% 125C 1206

U37
Gate Driver: NCP81075MTTXG Half Bridge 200V 4A WDFN10

Boot Cap: Establishes voltage 10V higher than Mosfet source
Z37B Zener: 15Vz 5% C .2W 100pF SOT23-3
C37B Cap: 0.47uF 100V 20% 125C 1206

Limit gate current to improve longevity.
Diode helps us turn off faster than turn on.
R37C Res: 100mOhm 5% .12W 1A 300ppm 0805
D37C Schottky: PMEG10010, 100V .8V-1A 4nS 70pF SOD123Wide

R37B
Res: 2.2ohm 5% 1W 400ppm 2512
1V/2.2ohm = 0.5A, 1W for 100nSec

GatePwr
10Vpwr
GatePwr_Left
10V, 100 to 200mA
VDD
HO
HB
HS
LI
LO
VSS_PAD
NC
NC2
HB_Left
HO_Left
GATE_Left_Hi
LO_Left
PCOM
FPGA_GateDrive_Left_Hi
FPGA_GateDrive_Left_Lo
From FPGA, LVC 3.3V, 2mA
1 = turns on Left_Lo/Left_Hi mosfet
RN37A Res4: 330ohm 50V 5% .06W 1206ve
RN37B Res4: 330ohm 50V 5% .06W 1206ve
330 protects IC if digital pwr appears before Vdd.
330 x 5pF = 2nS; 3V / 330 = 10mA, 30mW
3V / 33K = 100uA, 0.3mW
RN65B Res4: 33Kohm 50V 5% .06W 1206vex
RN65A Res4: 33Kohm 50V 5% .06W 1206vex
If both FPGA ctrl signals are 1 then you will short out PvPwr!

R37D Res: 1.5ohm 200V 1% .25W 200ppm 1206
R37E Res: 1.5ohm 200V 1% .25W 200ppm 1206
R37F
Res: 49.9Kohm 75V 1% .06W 100ppm 0603
Safety -- keep mosfet off if GateDriver pwr is down

PvPwr_Input
Drain
Left_HI Mosfet
Source
Inductor

This gate driver does not have lockout, which means you can turn on both mosfets at same time and short Pv to ground and burn out mosfets. Also, this means you can run experiments such as measuring mosfet Ron by shorting them when sun is low. Or measuring gate leakage current.

I need DCV 10V above src to Keep Mosfet always on (from gatepwr above)
I need DCV 10V above src to Keep Mosfet always on (from gatepwr above)
I need DCV 10V above src to Keep Mosfet always on (from gatepwr above)

Limit gate current to improve longevity.
Diode helps us turn off faster than turn on.
R40C Res: 100mOhm 5% .12W 1A 300ppm 0805
D40A Schottky: PMEG10010, 100V .8V-1A 4nS 70pF SOD123Wide

R40A Res: 1.5ohm 200V 1% .25W 200ppm 1206
R40B Res: 1.5ohm 200V 1% .25W 200ppm 1206

R40D
Res: 49.9Kohm 75V 1% .06W 100ppm 0603
Safety -- keep mosfet off if GateDriver pwr is down

Attach Inductor Left to COM via 33K ohm to bleed caps and measure mosfet Ron

GLLD Mofset bleeds current from node to left of main inductor to COM via 33K ohm. This is used to measure Cin capacitance, measure Left_HI Ron, and measure Left_LO mosfet Ron. This mosfet is turned on rarely.

InductorLeft_Pw+
R37G
Res: 33Kohm 200V 1% .25W 100ppm 1206
75V / 33K = 2.3mA, 170mW
50V / 33K = 1.5mA, 75mW
GLLD Mosfet
N-Ch
FPGA_BleedCurrent_Left
3V: turn on 33K ohm load
FPGA programmed for 8mA output, 3.3V LVC
M37
MOSFET: N-ch BSS123L 100V 6ohm SOT23
BSS123L, N-Chan, Sot23, 100V, 6O,
3Vgs th fully on, $0.04
PCOM

Isolate mosfet Left_Lo's Gate from it's Gate Driver so we can measure it's leakage current

GLB Mofset isolates Gate Driver from Left_Lo Gate, which enables us to measure the Left_Lo Gate leakage current, which enables us to know how long it will last.

We put o.o Volts drop (Vds) across GLB mosfet so gate leakage across it is o.o, so it does not effect our measurement of Left_Lo gate leakage.

GatePwr
10Vpwr
M38B
MOSFET: N/P Array DMC3400SDW 30V 500mOhm SOT363
DMC3400SDW: 3Vgs th, 50pF Ciss, 10uA Idss/Igss, $0.06
GLBU Mosfet: turns on GLB mosfet
GLBU mosfet
P-Ch
RN38B
Res4: 100Kohm 50V 5% .06W 1206vex
This R turns off GLBU mosfet by pulling Vgs to 0V
This R helps turn off GLB mosfet by pulling it's gate to 0V
10V / 330K = 30uA, 800uW
Res4: 330Kohm 50V 5% .06W 1206vex
RN64B
GLBD mosfet
N-Ch
FPGA_GLB_Control
3V: turns on GLB mosfet via GLBD & GLBU
and connects gate driver to Left_Lo gate
0V: turns off mosfet (isolate Left_Lo Gate from Gate Driver)
DN38B
Diode: 3x Array BAS16 100V 4pF 6nS SOT363
PCOM
M38A
MOSFET: N/P Array DMC3400SDW 30V 500mOhm SOT363
DMC3400SDW: 3Vgs th, 50pF Ciss, 10uA Idss/Igss, $0.06
GLBD Mosfet: turns on GLBU mosfet
RN63B
Res4: 10Kohm 50V 5% .06W 1206vex
10V / 110K = 90uA, 0.9mW
RN38C
Res4: 100Kohm 50V 5% .06W 1206vex
C38A
Cap: 0.01uF 50V 10% 125C 0603
Z38
Zener: 13Vz 5% C .2W 100pF SOT23-3
GLB Mosfet
N-Ch
M39
MOSFET: N-ch DMN6075S 60V 85mOhm SOT23
DMN6075S, 3.5Vgs th fully on, 20Vgs max, $0.06
GLB Mosfet: switches in GateDrive signal for Left_Lo mosfet.
GLB isolates Gate Driver from Left_Lo's Gate, so that we can measure Left_Lo Gate Leakage Current. GLB is always ON, except when you loose GatePwr (10V) or when Left_Lo is on for 10mSec or when you are doing Left_Lo leakage current testing.
When doing leakage current testing, GLB is closed, and GLHD (hold down) is off.

Measure Left_Lo mosfet gate leakage current

For simulation, see "Gate_Drv_Testing_UCC27282_2xFet_Switch_v14f.TSC"
For analysis and documentation, see " Analysis: GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "MOSFET Gate Leakage Current Measurement"

If you set MasterCal to 1500mV and Left_Lo gate leakage is 100pA, then you will get 100uV (100pA x 1M) across R_sense (1M) and then you will get 2200uV across R_gain (22M) and you will see 1502.2mV at op amp output and you will see 1499.9mV at R_sense input. Also, if you feed this into Main Amp input follower then you can compare this with 1500mV at 16bit a/d In+/In- differential input and multiply 2.2mV difference by a/d G=16 and see 2.2mV x 16 = 33mV different at A/D.

If you set MasterCal to 1500mV and Left_Lo gate leakage is 10nA, then you will get 10mV (10nA x 1M) across R_sense (1M) and then you will get 220mV across R_gain (22M) and you will see 1720mV at op amp output and you will see 1490mV at R_sense input. Also, if you feed this into Main Amp input follower then you can compare this with 1500mV at 16bit a/d In+/In- differential input and multiply 220mV difference by a/d G=1/2/4/8/16 as needed.

We use 1500mV since we want to have Left_Lo mosfet Vgs to be as large as possible. We use 16bit a/d differential input since it gets us G = 1/2/4/8/16. We calibrate system per notes in .xls file.

TLV2333 is very low leakage.

For analysis and documentation, see > Analysis: GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "MOSFET Gate Leakage Current Measurement"

U42A
OpAmp: TLV2333 2ch 350KHz 16uVos 125pA 102dB SO8
TLV2333, 2Ch, $1.12, 350KHz, 15uVos mx 25C,
125pA typ 125C, 16VuS, 102dB min,
In -.1V to (Vcc+0.1V), Out 100mV to (Vcc-100mV), SO-8

R42B
Res: 1Mohm 75V 1% .06W 100ppm 0603
If you set MasterCal to 0.1V and leakage is 10pA
then you will get 100pA x 1M = 100uV across 1M

R42A
Res: 22Mohm 150V 1% .1W 200ppm 0805
Gain = -22M / 1M = -22.0
~1.5V
4.3V_APwr
GateLeakageMeas_Left_Lo
1.5V...3.0V
Master_vCal_BUFF
~1.5V calibration voltage
This sets voltage at OpAmp IN- and IN+ pins
0V ...3.1V
Proportional to Left_Lo gate leakage current
Calibration: short Gate_left_Lo to gnd, set vCal to 100mV and look at op amp output.
For details, see .xls / "MOSFET Gate Leakage Current Measurement".
-1V_APwr
R42C
Res: 1Mohm 75V 1% .06W 100ppm 0603
This keeps Rsource same at IN- and IN+
Left_Lo Mosfet
Drain
Source
GATE_Left_Lo
PCOM

Pull Down mosfet Left_LO's gate to keep from lifting when Left_HI mosfet turns on. This is done during EVERY CONVERSION CYCLE.

GLHD Mosfet holds down the Left_Lo Gate while Left_Lo's Source moves fast (dV/dT) and pushes current into Left_Lo's Gate and lifts it, and turns it on.

The GateDvr pulls down gate via 3.o ohm Rseries (which limits gate current). This mosfet is after those R's, we hold it down via 9om ohm.

This mosfet is OFF during leakage test. It is only on for a moment while Left_Hi is slewing (turning on).

GLHD Mosfet
N-Ch
FPGA_GatePullDown_Left_LO
3V: short Left_Lo gate to 0V (hold it down)
FPGA output set for 16mA with 3.3Vpwr
R40E
Res: 100ohm 75V 1% .06W 100ppm 0603
100 ohm protects circuit from over-current.
1.4nC / 16mA = 1.4e-9 / 16e-3 = 90nSec
3V / 16mA = 187ohm Rsource from LVC 3.3V
(100ohm + 187ohm) x 130pF = 37nSec time constant
This lifts to 0.6V when GLHD Drain moves (due to Drain to Gate capacitance), which turn on (100mA drain current for 7nSec) yet this is a short time.
PCOM
M40
MOSFET: N-ch DMG2302UK 20V 80mOhm SOT23
DMG2302UK, N-Chan, $0.05, Sot23, 20Vds,
12Vgs, 90 mO, 1Vgs th, 130pF Ciss, 10uA
Idss/Igss, Built In Zeners

Maintain 0Volts across GLB mosfet during Left_Lo leakage test (to set GLB leakage to 0pA)

For simulation, see "Gate_Drv_Testing_UCC27282_2xFet_Switch_v14f.TSC"
For analysis, see: GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "MOSFET Gate Leakage Current Measurement"

RN41A
Res4: 47Kohm 50V 5% .06W 1206vex
Max: 10V / 50K = 200uA, 2mW
Note: if op amp goes high by 0.6V it will turn on GLB internal diode.
U42B
OpAmp: TLV2333 2ch 350KHz 16uVos 125pA 102dB SO8
VERY LOW LEAKAGE OP AMP
4.3V_APwr
RN41B
Res4: 47Kohm 50V 5% .06W 1206vex
Max: 10V / 50K = 200uA, 2mW
RN41C
Res4: 47Kohm 50V 5% .06W 1206vex
(10V-5V) / 50K = 100uA, 0.5mW
50pA x 50K = 50e-12 x 50e3 = 2.5uVos
-1V_APwr
C41A
Cap: 1000pF 50V 10% 125C 0603
50K, 50K and 1nF enable op amp to drive capacitive loads
C41B
Cap: 0.01uF 50V 10% 125C 0603
Reduce noise from uProcessor
50k x 10nF = 500uS, 350Hz
PCOM

This op amp is ONLY used to help measure leakage current of Left_Lo mosfet's gate. Also, this op amp ONLY does one thing, which is detects mosfet GLB Drain voltage and then drives GLB Source with that same voltage. This cause Vds (voltage across mosfet) to be o.oV. This causes leakage current across GLB to be o.opA. This means measured leakage is only coming from Left_Lo gate (and not it's driver).

Supply HO_Left Gate Power when Buck is OFF and Boost is ON

(Vout + 10V)
HB_Right
(Vout)
Vout_Pwr+
D37R Diode: BAS21 200V 5pF 50nS SOT23-3
D37S Diode: BAS21 200V 5pF 50nS SOT23-3
BAS21L, $0.02, 1x, sot23, 250V, 5pF, 50nS, 0.2uA/100V/85C
R37S
Res: 100Kohm 200V 1% .25W 100ppm 1206
50V / 100K ohm = 0.5mA, 25mW
2K pF x 100K ohm = 200uSec TC
HB_Right

```
Example:
 * Buck Converter OFF, Boost Converter ON
 * Vin = 30V
 * Vout = 60V = Inductor_Right
 * GatePwr = 10V
 * HB_Right = square wave 10V to 70V
  * Inductor_Right = square wave 0V to 60V (Right HI Mosfet Source)
 * 100K ohm Path from Vout (60V) and HB_Right (70V), to Mosfet HI Left Gate
```

Title			www.Manhattan2.org
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Date: 11/30/2020	Time: 12:12:19 PM	Sheet of	
File: C:\Users\glenn\Documents\GWT\gw\...\Dev\Net-4xx 2004 Design\Projects\...\m100_GateDrive_Left.SchDoc			Designed by: GWeinreb 2020 for m100

Gate Drive: Right of Main Inductor (i.e. drive gates of Right_Lo and Right_Hi mosfets)

For simulation, see "Gate_Drv_Testing_UCC27282_2xFet_Switch_v14f.TSC"
For simulation, see GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "Buck Converter Math"
ALL COLUMNS HAVE THIS

Input Filter
0.3 ohm x 10uF = 3 uSec, 20 KHz Fc
PEAK: 0.3A x 0.3 ohms = 100mV, 30mW
AVG: 0.2A x 0.3 ohms = 66mV, 12mW

R43A Res: 330mOhm 5% .06W .4A 300ppm 0603
C43A Cap: 10uF 25V 20% 125C 1206

U43
Gate Driver: NCP81075MTTXG Half Bridge 200V 4A WDFN10

GatePwr
10Vpwr
PCOM
GatePwr_Right 10V, 100 to 200mA
VDD HO
HB
HI HS
LI
LO
VSS NC
VSS_PAD NC2
HO_Right
LO_Right
FPGA_GateDrive_Right_Hi
FPGA_GateDrive_Right_Lo
From FPGA, LVC 3.3V, 2mA
1 = turns on Right_Lo / Right_Hi mosfet

RN37C Res4: 330ohm 50V 5% .06W 1206ve
RN37D Res4: 330ohm 50V 5% .06W 1206ve
330 protects IC if digital pwr appears before Vdd.
330 x 5pF = 2nS; 3V / 330 = 10mA, 30mW
3V / 33K = 100uA, 0.3mW

RN65C Res4: 33Kohm 50V 5% .06W 1206vex
RN65D Res4: 33Kohm 50V 5% .06W 1206vex
If both FPGA ctrl signals are 1 then you will short out PvPwr !

This gate driver does not have lockout, which means you can turn on both mosfets at same time and short Pv to ground and burn out mosfets. Also, this means you can run experiments such as measuring mosfet Ron by shorting them when sun is low. Or measuring gate leakage current.

Boot Cap: Establishes voltage 10V higher than Mosfet source
Z43B Zener: 15Vz 5% C .2W 100pF SOT23-3
C43B Cap: 0.47uF 100V 20% 125C 1206

Limit gate current to improve longevity.
Diode helps us turn off faster than turn on.
R43C Res: 100mOhm 5% .12W 1A 300ppm 0805
D43C Schottky: PMEG10010, 100V .8V/1A 4nS 70pF SOD123Wide

R43B
Res: 2.2ohm 5% 1W 400ppm 2512
1V/2.2ohm = 0.5A, 1W for 100nSec

HB_Right
R43D Res: 1.5ohm 200V 1% .25W 200ppm 1206
R43E Res: 1.5ohm 200V 1% .25W 200ppm 1206
GATE_Right_Hi
InductorRight_Pwr+
R43F
Res: 49.5Kohm 75V 1% .06W 100ppm 0603
Safety – keep mosfet off if GateDriver pwr is down
Inductor
Source
Drain
Vout
Right_Hi Mosfet

Limit gate current to improve longevity.
Diode helps us turn off faster than turn on.
R43G Res: 100mOhm 5% .12W 1A 300ppm 0805
D43E Schottky: PMEG10010, 100V .8V/1A 4nS 70pF SOD123Wide

R43H Res: 1.5ohm 200V 1% .25W 200ppm 1206
R43L Res: 1.5ohm 200V 1% .25W 200ppm 1206
GATE_Right_Lo
Drain
Source
Right_Lo Mosfet
PCOM
R43K
Res: 49.9Kohm 75V 1% .06W 100ppm 0603
Safety – keep mosfet off if GateDriver pwr is down

I need DCV 10V above src to Keep Mosfet always on (from gatepwr above)
I need DCV 10V above src to Keep Mosfet always on (from gatepwr above)
I need DCV 10V above src to Keep Mosfet always on (from gatepwr above)

Pull Down mosfet Right_Lo's gate to keep from lifting when Right_Hi mosfet turns on. This is done during EVERY CONVERSION CYCLE.

GRHD Mosfet
N-Ch
FPGA_GatePullDown_Right_Lo
3V: short Right_Lo gate to 0V (hold it down)
FPGA output set for 16mA with 3.3Vpwr

R43M
Res: 100ohm 75V 1% .06W 100ppm 0603
100 ohm protects circuit from over-current.
1.4nC / 16mA = 1.4e-9 / 16e-3 = 90nSec
3V / 16mA = 187ohm Rsource from LVC 3.3V
(100ohm + 187ohm) x 130pF = 37nSec time constant
This lifts to 0.6V when GRHD Drain moves (due to Drain to Gate capacitance), which turn on (100mA drain current for 7nSec) yet this is a short time.
PCOM

GRHD Mosfet holds down the RightLo Gate while Right_Lo's Source moves fast (dV/dT) and pushes current into Right_Lo's Gate and lifts it, and turns it on.

The GateDvr pulls down gate via 3.0 ohm Rseries (which limits gate current). This mosfet is after those R's, we hold it down via 90m ohm.

This mosfet is OFF during leakage test. It is only on for a moment while Right_Hi is slewing (turning on).

M43A
MOSFET: N-ch DMG2302UK 20V 90mOhm SOT23
DMG2302UK, N-Chan, $0.05, Sot23, 20Vds, 12Vgs, 90 mO, 1Vgs th, 130pF Ciss, 10uA Idss/Igss, Built In Zeners

Attach Inductor Right to COM via 33K ohm to bleed caps and measure mosfet Ron

GRLD Mofset bleeds current from node to right of main inductor to COM via 33K ohm. This is used to measure Cin capacitance, measure Right_Hi Ron, and measure Right_Lo mosfet Ron. This mosfet is turned on rarely.

InductorRight_Pwr+
R43P
Res: 33Kohm 200V 1% .25W 100ppm 1206
75V / 33K = 2.3mA, 170mW
50V / 33K = 1.5mA, 75mW
GRLD Mosfet
N-Ch
FPGA_BleedCurrent_Right
3V: turn on 33K ohm load
FPGA programmed for 8mA output, 3.3V LVC
PCOM

M43B
MOSFET: N-ch BSS123L 100V 6ohm SOT23
BSS123L, N-Chan, Sot23, 100V, 6O,
3Vgs th fully on, $0.04

Supply HO_Right Gate Power when Buck is ON and Boost is OFF

(Vin + 10V)
HB_Left
(Vin)
PvPwr_Filtered+

D43R Diode: BAS21 200V 5pF 50nS SOT23-3
D43S Diode: BAS21 200V 5pF 50nS SOT23-3
BAS21L, $0.02, 1x, sot23, 250V, 5pF, 50nS, 0.2uA/100V/85C

R43S
Res: 100Kohm 200V 1% .25W 100ppm 1206
50V / 100K ohm = 0.5mA, 25mW
2K pF x 100K ohm = 200uSec TC
HB_Right

```
Example:
 * Buck Converter ON, Boost Converter OFF
 * Vin = 60V
 * GatePwr = 10V
 * HB_Left = square wave 10V to 70V
 * Vout = 20V = Inductor_Right
 * Inductor_Left = square wave 0V to 60V (Left HI Mosfet Source)
 * 100K ohm Path from Vin (60V) and HB_Left (70V), to Mosfet HI Right Gate
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Title			
Size: Letter	Number:	Revision:	
Date: 11/30/2020	Time: 12:12:19 PM	Sheet of	
File: C:\Users\glenn\Documents\GWI\gwi_Dev\iNet-4xx 2004 Design\Designs\m100\m100_SchPcb_CurrentWorkingFiles\Schematics\m100 Specific\m100_GateDrive_Right.SchDoc			

Manage GatePwr in String of PCB's

COLUMN #1 ONLY

GatePwr in PCB above me in string (higher voltage)
This is 10V (GatePwr) + my Vout
15V DC-to-DC Converter at end of entire string

DESIGN FILES
> Simulation: "ByPass_Mosfet_v3a.TSC"
> Analysis: GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "GatePwr (10V) AboveMe Circ

CIRCUIT OBJECTIVES
> If no power appears in this array element, GatePwr (e.g. 10V) from Above element in string powers bypass MOSFET, which puts 0.004 ohms across string (instead of broken string).
> If there is no PV power to entire string, then 5V-to-15V dc/dc converter at end of string (near ideal diode) puts 15V into string, which should turn on all ByPass MOSFETS, which pulls all elements in string to earth ground, which is safer.
> If my local GatePwr (e.g. 10V) does not turn on (e.g. no PV power), then i still need to transfer the GatePwr_AboveMe (next element in string) to the GatePwr_BelowMe (previous element in string). We do this via the ConnectToGatePwrAboverMe MOSFET, which turns on automatically if our element has no power.
> If there is no GatePwr_AboveMe power, then my local GatePwr (10V from PV) might supply the string element below me (GatePwr_BelowMe).
> 18V Zener "LimitTo20V" limits GatePwr_BelowMe to <20V.
> 30V Zener "30VsafetY" limits GatePwr_BelowMe to <30V, as an additional safety measure.
> It is our intent to get GatePwr (10V) via our own local power (1st choice), or if our PV power is down, we get it from the string element above us (2nd choice). We are Not intending to pass the GatePwr (10V) above us when we are creating voltage at our element position, causing that GatePwr to be (10V + OurVoutVoltage) which might be 90V. The ConnectToGatePwrAboverMe mosfet opens if we try to do that, and limits the passed voltage to 20V.
> This limiter sometimes oscillates, yet this is ok since this is not an operating scenario (GatePwr_AboveMe should not be passed below when we have PV power). Limiters are safety only.

DISCOVERY OF EACH ELEMENT WITHIN ONE STRING
> Discovery involves each element determining its own position within the string. We do this by first turning off all PV power and also all GatePwr (e.g. in factory), then last element in string has 5V-to-15V converter which turns on all ByPass mosfets via 0.6Vdrop diodes (8 x .6V = 4.8V), and first element in string loads down the 12V diode string via the 20K resistor and "LoadGatePwr" MOSFET. We measure diode string voltages with a/d to see position in string.

COMMUNICATING WITH STRING NEIGHBOR VIA FPGA DOUT BIT
> If you turn off PV power, turn off GatePwr, have 5V-to-15V dc-to-dc at end of string push 15V into GatePwr_AboveMe, turn on 20K load at bottom of string via "LoadGatePwr" MOSFET, then you will have low 0 to 15V voltages along the string. You can then turn on/off ConnectToGatePwrAboverMe MOSFET and measure these voltages to communicate a 0 and 1 between neighbors in the string. There is no reason to do this, yet i think this is possible.

GatePwr_AboveMe

0 to 100V (Vout + 10V)
COLUMN #1 ONLY

(100 // 100) + (100 // 100) = 100 ohms total
30mA x 100 ohms = 3Vdrop, 90mWatts -- very rare

RN44A Res4: 100ohm 50V 5% .06W 1206ve
RN44B Res4: 100ohm 50V 5% .06W 1206ve

RN44C Res4: 100ohm 50V 5% .06W 1206ve
RN44D Res4: 100ohm 50V 5% .06W 1206ve

D44A
Diode: BAS21 200V 5pF 50nS SOT23-3
BAS21L, $0.02, 1x, sot23, 250V, 5pF, 50nS, 0.2uA/100V/85C
85V + 10V = 95V max

GatePwr_AboveMe_Safer

A/D Voltage Measurement, 10V to +135V measurement (Vout + 10V)
PCB above me can turn it's GatePwr (10V) on or off via it's FPGA
and i can detect this w/ a/d and therefore communicate w/ pcb above me in string.

M44C
MOSFET: P-ch BSS84PH 60V 8ohm SOT23
BSS84PH, P-Chan, Sot23, 60V, 8O, 3.5Vgs th fully on, $0.04

M44A
MOSFET: P-ch BSR92PH 250V 20ohm SOT23
BSR92PH, P-Chan, $0.15, Sot23, 250V, 20ohms, 3Vgs th fully

Zener: 13Vz 5% C .2W 100pF SOT23-3
Z44A

75V + 10V = 85V

R44A
Res: 100Kohm 150V 1% .1W 100ppm 0805

AboveMe_CtrlHi Mosfet
10V_AboveMe is always ON unless this mosfet turns it OFF.

Z44F
Zener: 13Vz 5% C .2W 100pF SOT23-3
BZX84C13LT1G, 13Vz, 5% C, 100pF, .2W, Sot23, OFF
8V@100nA/25C, ON 14.2V@20mA/25C, $0.02

R44C
Res: 330Kohm 150V 1% .1W 100ppm 0805

GatePwr 10Vpwr

D44B
Diode: BAS21 200V 5pF 50nS SOT23-3
BAS21L, $0.02, 1x, sot23, 250V, 5pF, 50nS, 0.2uA/100V/85C

R44B
Res: 100Kohm 150V 1% .1W 100ppm 0805
Typ: 10V / 100K = 100uA, 1mW
Max: 75V / 100K = 750uA, 50mW

85V (OFF) or 80V (ON)

75V + 10V - 13V = 72V

R44D
Res: 330Kohm 150V 1% .1W 100ppm 0805

ConnectToGatePwrAboverMe MOSFET

Output Power+ (e.g. 75V)

Vout_Pwr+

DN40A
Diode: 3x Array BAS16 100V 4pF 6nS SOT363

This is typically 9.6V (GatePwr - 0.4V) or GatePwrAboveMe (14V) This limits GatePwr_MeOrAboveMe to 20V (safety only)

Z44C
Zener: 13Vz 5% C .2W 100pF SOT23-3
BZX84C13LT1G, 13Vz, 5% C, 100pF, .2W, Sot23, OFF
8V@100nA/25C, ON 14.2V@20mA/25C, $0.02

GatePwr_MeOrAboveMe

My GatePwr (10V) or PCB above me's GatePwr (14V)
Typically 10V yet max could be 28V while configuring.
If my GatePwr is up then this signal is (GatePwr - 0.4Vdiode);
otherwise, this is PCB above me's GatePwr minus
his diode + 100 ohm + Mosfet.

Z44B
Zener: 30Vz 5% C .2W 100pF SOT23-3
Safety, keeps < 30V no matter what
Also, keeps this node > -0.6V

PCOM

FPGA_TurnOff10VaboveMe

LVC 3.3V (logic 0 = 0.4V, logic 1 = 2.8V)
1 = Fpga turns OFF GatePwr_AboveMe
0 = Fpga turns ON GatePwr_AboveMe
COLUMN #1 ONLY
RN45A
Res4: 47Kohm 50V 5% .06W 1206vex

Z44D
Zener: 15Vz 5% C .2W 100pF SOT23-3
15V zener

M44D
MOSFET: N-ch BSS123L 100V 6ohm SOT23
BSS123L, N-Chan, Sot23, 100V, 6O,
3Vgs th fully on, $0.04

AboveMe_CtrlLo MOSFET
Turn ON this fet to turns OFF GatePwr_AboveMe

Z44E
Zener: 13Vz 5% C .2W 100pF SOT23-3

GatePwr 10Vpwr

RN45C Res4: 47Kohm 50V 5% .06W 1206vex
RN45D Res4: 47Kohm 50V 5% .06W 1206vex
47K // 47K = 23.5K
30 Volts / 20 K ohm = 1.5mA, 45mW across this resistor
1.5mA x 75V = 112mW across Mosfet
30V is very rare, 10V is more typical.

R44E
Res: 10ohm 75V 1% .06W 100ppm 0603

LoadGatePwr MOSFET

FPGA_LoadDown_MeOrAboveMe

1 = fpga loads down MeOrAboveMe via 20K ohm
This can signal above PCB.
This can help drain capacitors for safety.
This can help w/ testing.
COLUMN #1 ONLY
M44B
MOSFET: N-ch BSS123L 100V 6ohm SOT23
BSS123L, N-Chan, Sot23, 100V, 6O, 3Vgs th fully on,

Res4: 47Kohm 50V 5% .06W 1206vex
RN45B

PCOM

GatePwr_BelowMe

PCB below me in string (lower voltage)
This powers mosfet gates in PCB below me.
COLUMN #1 ONLY

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HiPwrOn SOURCE (aka "Emergency Shutdown", "System Reset")

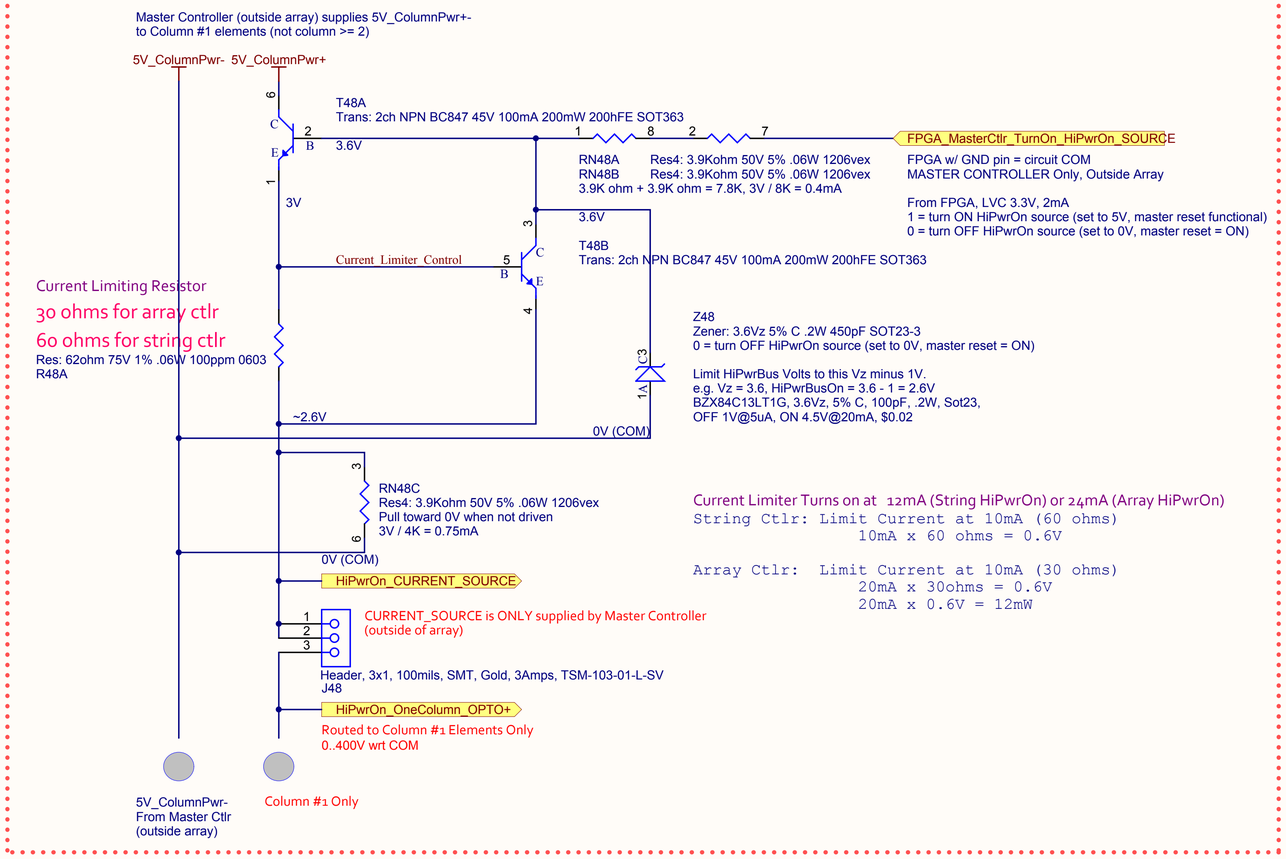
> Any element can initiate emergency shutdown of other elements in the array
> Helps to mitigate fire risk when solar is placed near plywood
> External switch enables fire dept to shut down system.

MASTER CONTROLLER ONLY (outside of array)

DESIGN FILES

> Simulation: "SystemMasterReset_HiPwrOn_OptoCoupler_11a.TSC"
> Analysis: GWeinreb_Manhattan2_ResearchNotes.xls 7 SolarRoof / "HiPwrOn (similar System Master Reset) .."

Master Controller, HiPwrOn Current SOURCE, 10 or 20mA, 3V



Current Limiter Turns on at 12mA (String HiPwrOn) or 24mA (Array HiPwrOn)

```
String Ctlr: Limit Current at 10mA (60 ohms)
             10mA x 60 ohms = 0.6V

Array Ctlr:  Limit Current at 10mA (30 ohms)
             20mA x 30ohms = 0.6V
             20mA x 0.6V = 12mW
```

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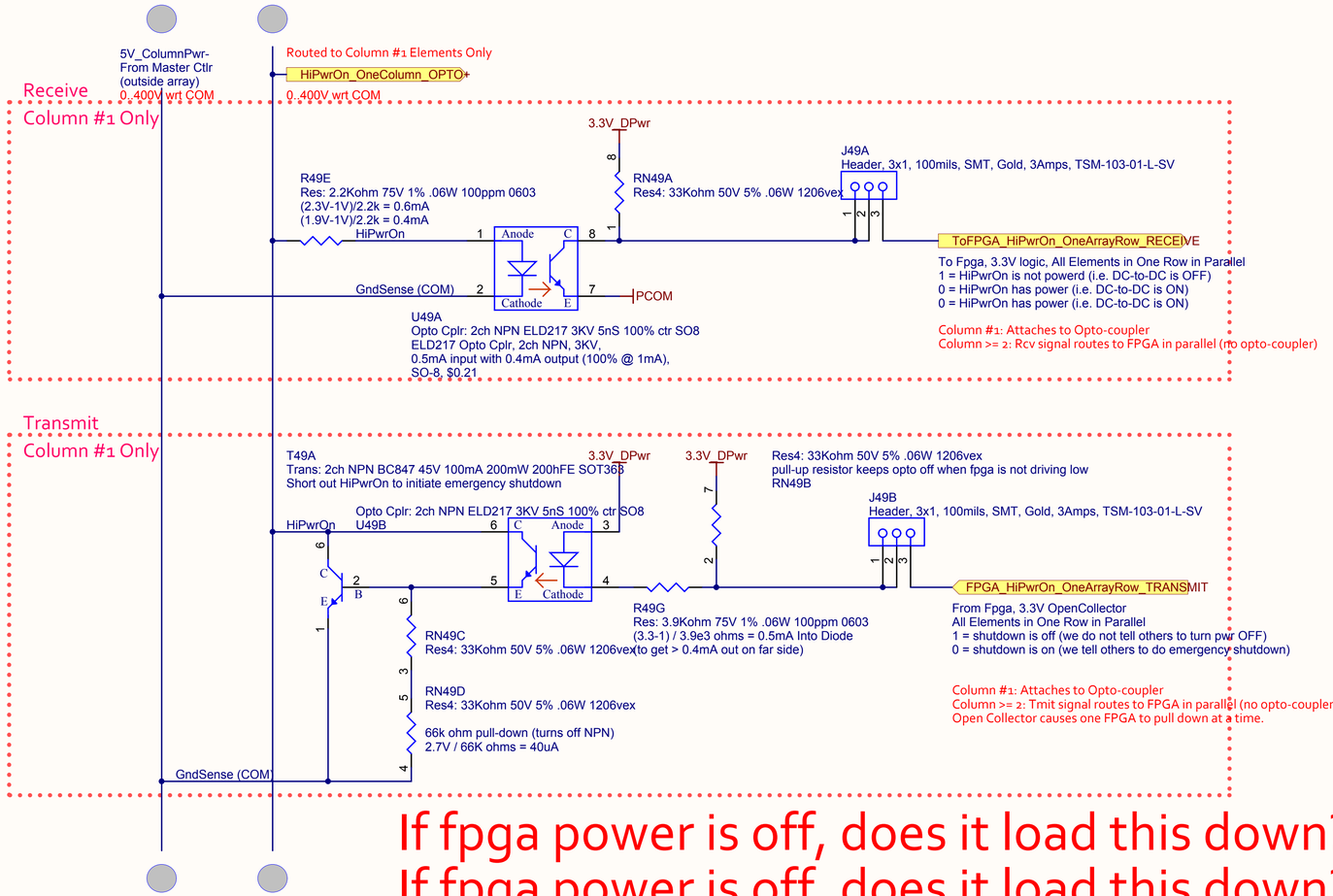
HiPwrOn Transmit/Receive (aka "Emergency Shutdown", "System Reset"))

> Any element can initiate emergency shutdown of other elements in the array
> Helps to mitigate fire risk when solar is placed near plywood
> External switch enables fire dept to shut down system.
COLUMN #1 ONLY

DESIGN FILES
> Simulation: "SystemMasterReset_HiPwrOn_OptoCoupler_11a.TSC"
> Analysis: GWeinreb_Manhattan2_ResearchNotes.xls 7 SolarRoof / "HiPwrOn (similar System Master Reset) ..."



If fpga power is off, does it load this down?

If fpga power is off, does it load this down?

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Main Voltage Measurement Amplifier

For Mathematical Analysis, see "Amplifier_400V_SE_1MHz_Mux_Between_Rg-Rfb...TSC"
ALL COLUMNS HAVE THIS

SUMMARY

" Main Voltage Measurement
> Supports measuring high voltages
> Very precise

DESIGN FILES

```
> Simulation: "Amplifier_400V_SE_1MHz_Mux_Between_Rg-Rfb...TSC"
 > Analysis:   GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "DESIGN: Measure High Volt via Inverting Op-Amp...", "Power and Voltage Range Strategy...", "Current and Voltage Measurements", "Component Characteristics As Noted in Datasheets"
 > Ma2_Solar_RD_PLAN.pdf / "Voltages are prepared for Measurement"
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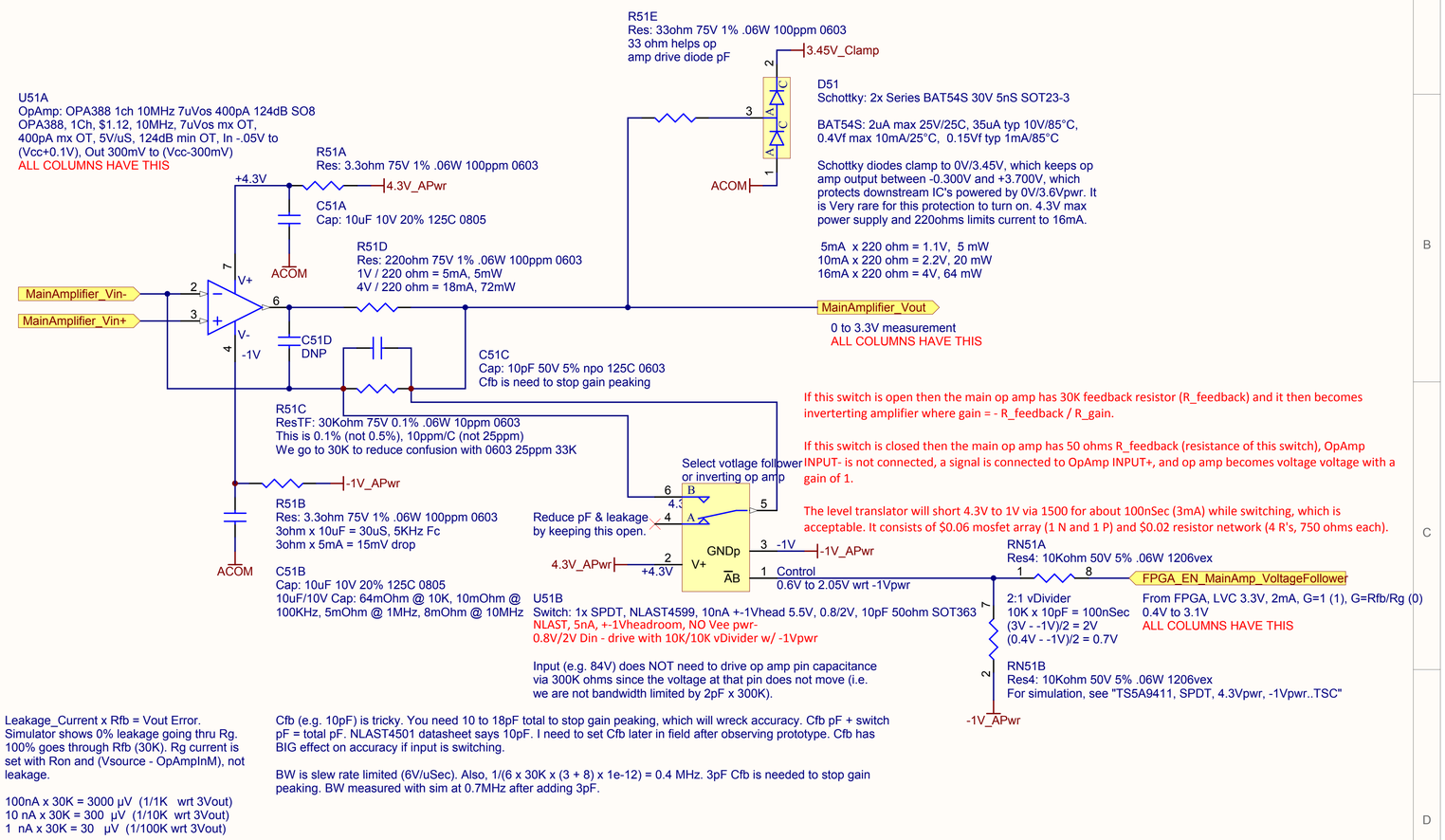

If this switch is open then the main op amp has 30K feedback resistor (R_feedback) and it then becomes inverterting amplifier where gain = - R_feedback / R_gain.

If this switch is closed then the main op amp has 50 ohms R_feedback (resistance of this switch), OpAmp INPUT- is not connected, a signal is connected to OpAmp INPUT+, and op amp becomes voltage voltage with a gain of 1.

The level translator will short 4.3V to 1V via 1500 for about 100nSec (3mA) while switching, which is acceptable. It consists of $0.06 mosfet array (1 N and 1 P) and $0.02 resistor network (4 R's, 750 ohms each).

Leakage_Current x Rfb = Vout Error.
Simulator shows 0% leakage going thru Rg. 100% goes through Rfb (30K). Rg current is set with Ron and (Vsource - OpAmpInM), not leakage.

100nA x 30K = 3000 µV (1/1K wrt 3Vout)
10 nA x 30K = 300 µV (1/10K wrt 3Vout)
1 nA x 30K = 30 µV (1/100K wrt 3Vout)

Cfb (e.g. 10pF) is tricky. You need 10 to 18pF total to stop gain peaking, which will wreck accuracy. Cfb pF + switch pF = total pF. NLAST4501 datasheet says 10pF. I need to set Cfb later in field after observing prototype. Cfb has BIG effect on accuracy if input is switching.

BW is slew rate limited (6V/uSec). Also, 1/(6 x 30K x (3 + 8) x 1e-12) = 0.4 MHz. 3pF Cfb is needed to stop gain peaking. BW measured with sim at 0.7MHz after adding 3pF.

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MAIN MULTIPLEXOR -- BANK 6 -- Voltage Follower

For Mathematical Analysis, see "Amplifier_400V_SE_1MHz_Mux_Between_Rg-Rfb...TSC"

ALL COLUMNS HAVE THIS

DESIGN FILES

> Simulation: "Amplifier_400V_SE_1MHz_Mux_Between_Rg-Rfb...TSC"
> Analysis: GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "DESIGN: Measure High Volt via Inverting Op-Amp...", "Power and Voltage Range Strategy...", "Current and Voltage Measurements", "Component Characteristics As Noted in Datasheets"
> Ma2_Solar_RD_PLAN.pdf / "Voltages are prepared for Measurement"

SUMMARY

> Main Voltage Measurement
> Supports measuring high voltages
> Very precise

2.81Vref_BUFFERED_Col_N — Each column has one of these.

Many measurements are wrt this 2.81V
Need buffer to avoid crosstalk through 8:1 mux
2.81V

On simulation, we see 1/1000 leak with 100nSec rise time and 50 ohm R_source.
Since these are buffered (low Rsource), we do not need to worry about crosstallk.
Reference: "scdm216, Crostalk Tests, v1.tsc"

ALL COLUMNS HAVE THIS
50nA, pin 7 n/c, pin 11 = A, 19%/25% Din, Drive w 10k // 10K divider & -1Vpwr, $0.15
Mux: 8:1, TMUX1308, 45nA +-1Vhead 5.5V, 19%/25%, 11pF 220ohm TSSOP16
U27A

MuxFollower_Bank7_OUTPUT	ALL COLUMNS	2.81V	4
vMeasure_FromAdjacentElement	0 to 3V measurement, ALL COLUMNS		12
Measure_7x_CurrentShunts_1.5MHz_BW	0 to 3V, 115mV/Amp with 1m ohm shunt, ALL COLUMNS		5
Measure_7x_CurrentShunts_16KHz_BW	0 to 3V, 115mV/Amp with 1m ohm shunt, ALL COLUMNS		14
Measure_Vout_5MHz_BW	0 to 3V measurement, ALL COLUMNS		2
			15
COLUMN #1 ONLY			1
ZERO_20mA	ALL COLUMNS		13

U27A: Y7 OUT 3 — Y6 — Y5 — Y4 — Y3 — Y2 — Y1 — Y0 — C 9 — B 10 — A 11 — Low = On ENABLE 6 — N/C — GNDp 7 — 8 — V+ 16

0V when not used

-1V: 7 — -1V_APwr

4.3V: 16 — 4.3V_APwr

Provide +-1V headroom via -1V/4.3Vpwr
19% / 25% digital inputs receive:
Logic 1: 1.96V wrt pin8 > [25% x (4.3V - -1V) = 1.38V]
Logic 0: 0.66V wrt pin8 < [19% x (4.3V - -1V) = 1.05V]

ALL COLUMNS
MainAmplifier_Vin+ → Main Amplifier (+ / -, 30K)

RN27A / RN27B	Res4: 10Kohm 50V 5% .06W 1206vex	1 — 8 — MuxFollower_Bank6_M2
	From FPGA, LVC 3.3V, 2mA	7 — 2 — -1V_APwr
RN27C / RN27D	Res4: 10Kohm 50V 5% .06W 1206vex	3 — 6 — MuxFollower_Bank6_M1
		5 — 4 — -1V_APwr
RN71A / RN71B	Res4: 10Kohm 50V 5% .06W 1206vex	1 — 8 — MuxFollower_Bank6_M0
		7 — 2 — -1V_APwr
RN71C / RN71D	Res4: 10Kohm 50V 5% .06W 1206vex	3 — 6 — MuxFollower_Bank6_ENABLE
	From FPGA, LVC 3.3V, 2mA, 0 = ON	5 — 4 — -1V_APwr

8:1 MUX
COLUMN #1 ONLY

Col_2_MainAmp_Output
Col_3_MainAmp_Output
Col_4_MainAmp_Output
Col_5_MainAmp_Output

Spikes on ACOM between Columns will cause vMeas error at Col >= 2.
ACOM, MasterCal_Buf, 2.81Vcal, etc. needs to be shielded between layers.
Need to do all calibration with GatePwr off and no pwr switching.
2.81v is connected to ACOM via cap -- Need this stable during power conversion?!
Need ACOM stable between columns during pwr conversion!?

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MAIN MULTIPLEXOR -- BANK 7 -- Voltage Follower

For Mathematical Analysis, see "Amplifier_400V_SE_1MHz_Mux_Between_Rg-Rfb...TSC"

ALL COLUMNS HAVE THIS

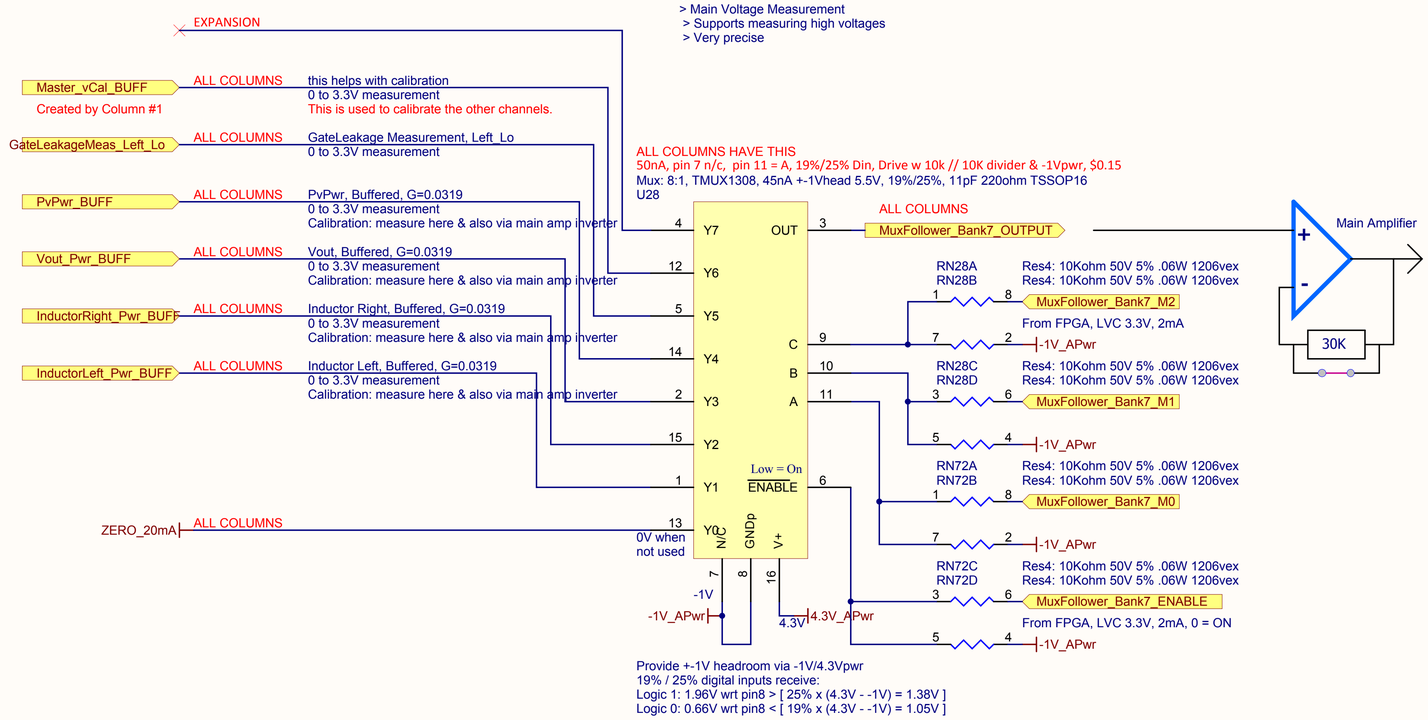
DESIGN FILES

> Simulation: "Amplifier_400V_SE_1MHz_Mux_Between_Rg-Rfb...TSC"
 > Analysis: GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "DESIGN: Measure High Volt via Inverting Op-Amp...", "Power and Voltage Range Strategy...", "Current and Voltage Measurements", "Component Characteristics As Noted in Datasheets"
 > Ma2_Solar_RD_PLAN.pdf / "Voltages are prepared for Measurement"

Since these are buffered (low Rsource), we do not need to worry about crosstallk.
On simulation, we see 1/1000 leak with 100nSec rise time and 50 ohm R_source.
Reference: "scdm216, Crostalk Tests, v1.tsc"

SUMMARY

> Main Voltage Measurement
 > Supports measuring high voltages
 > Very precise



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MAIN MULTIPLEXOR -- BANK 1 -- Inverting Input Channels

For Mathematical Analysis, see "Amplifier_400V_SE_1MHz_Mux_Between_Rg-Rfb...TSC"

ALL COLUMNS HAVE THIS

NLAST, 5nA, +-1Vheadroom, NO Vee pwr-, 0.8V/2V Din - drive with 10K/10K vDivider w/ -1Vpwr, $0.11/1ch

DESIGN FILES

> Simulation: "Amplifier_400V_SE_1MHz_Mux_Between_Rg-Rfb...TSC"
 > Analysis: GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "DESIGN: Measure High Volt via Inverting Op-Amp...", "Power and Voltage Range Strategy...", "Current and Voltage Measurements", "Component Characteristics As Noted in Datasheets"
 > Ma2_Solar_RD_PLAN.pdf / "Voltages are prepared for Measurement"

SUMMARY

> Main Voltage Measurement
 > Supports measuring high voltages
 > Very precise

Channel 1 (U20A)

1M ohm ResTF: 1Mohm 150V 0.5% .12W 25ppm 1206
R20A
Vout_Pwr+
ALL COLUMNS
Primary Dc-to-Dc Converter Output
-2V to 85V, Gain = -0.030, Vout = 2.81 - (Vin x 0.030)
Place 1M R close to Spdt, place Spdt close to 8:1 mux
ACOM
4.3V_APwr
U20A
Switch: 1x SPDT, NLAST4599, 10nA +-1Vhead 5.5V, 0.8/2V, 10pF 50ohm SOT363

-2V to 85V Ampln, Gain = -0.030 = -30K/1M, AmpOut = 2.81V - (Ampln x 0.030)
85V / 1M = 85uA. 85V x 85uA = 6mW. 20nA x 1M = 20mV error
2:1 vDivider (10K ohm, 10K ohm) converts FGPA 0.4V/3.05V to 0.7V/2.02V
Dout Control from FPGA, 1 = enable
-1V_APwr
RN20A
Res4: 10Kohm 50V 5% .06W 1206vex
FPGA_EN_Vout_Pwr+
0.7V to 2V
RN20B
Res4: 10Kohm 50V 5% .06W 1206vex
-1V_APwr

Channel 2 (U20B)

1M ohm ResTF: 1Mohm 150V 0.5% .12W 25ppm 1206
R20B
PvPwr_Panel+
ALL COLUMNS
PV Power+ (solar panel out)
-2V to 85V
Place 1M R close to Spdt, place Spdt close to 8:1 mux
ACOM
4.3V_APwr
U20B
Switch: 1x SPDT, NLAST4599, 10nA +-1Vhead 5.5V, 0.8/2V, 10pF 50ohm SOT363

-2V to 85V Ampln, Gain = -0.030 = -30K/1M, AmpOut = 2.81V - (Ampln x 0.030)
85V / 1M = 85uA. 85V x 85uA = 6mW. 20nA x 1M = 20mV error
2:1 vDivider (10K ohm, 10K ohm) converts FGPA 0.4V/3.05V to 0.7V/2.02V
Dout Control from FPGA, 1 = enable
-1V_APwr
RN20C
Res4: 10Kohm 50V 5% .06W 1206vex
FPGA_EN_PV_Pwr+
0.7V to 2V
RN20D
Res4: 10Kohm 50V 5% .06W 1206vex
-1V_APwr

Channel 3 (U20C)

1M ohm ResTF: 1Mohm 150V 0.5% .12W 25ppm 1206
R20C
PvPwr_Filtered+
ALL COLUMNS
Filter Output (after PV Input)
-2V to 85V
Place 1M R close to Spdt, place Spdt close to 8:1 mux
ACOM
4.3V_APwr
U20C
Switch: 1x SPDT, NLAST4599, 10nA +-1Vhead 5.5V, 0.8/2V, 10pF 50ohm SOT363

-2V to 85V Ampln, Gain = -0.030 = -30K/1M, AmpOut = 2.81V - (Ampln x 0.030)
85V / 1M = 85uA. 85V x 85uA = 6mW. 20nA x 1M = 20mV error
2:1 vDivider (10K ohm, 10K ohm) converts FGPA 0.4V/3.05V to 0.7V/2.02V
Dout Control from FPGA, 1 = enable
-1V_APwr
RN21A
Res4: 10Kohm 50V 5% .06W 1206vex
FPGA_EN_FiltrOut_Pwr+
0.7V to 2V
RN21B
Res4: 10Kohm 50V 5% .06W 1206vex
-1V_APwr

Channel 4 (U20D)

1M ohm ResTF: 1Mohm 150V 0.5% .12W 25ppm 1206
R20D
InductorLeft_Pwr+
ALL COLUMNS
Primary Inductor Input Side
-2V to 85V
Place 1M R close to Spdt, place Spdt close to 8:1 mux
ACOM
4.3V_APwr
U20D
Switch: 1x SPDT, NLAST4599, 10nA +-1Vhead 5.5V, 0.8/2V, 10pF 50ohm SOT363

-2V to 85V Ampln, Gain = -0.030 = -30K/1M, AmpOut = 2.81V - (Ampln x 0.030)
85V / 1M = 85uA. 85V x 85uA = 6mW. 20nA x 1M = 20mV error
2:1 vDivider (10K ohm, 10K ohm) converts FGPA 0.4V/3.05V to 0.7V/2.02V
Dout Control from FPGA, 1 = enable
-1V_APwr
RN21C
Res4: 10Kohm 50V 5% .06W 1206vex
FPGA_EN_InductorLeft_Pwr+
0.7V to 2V
RN21D
Res4: 10Kohm 50V 5% .06W 1206vex
-1V_APwr

Channel 5 (U20E)

1M ohm ResTF: 1Mohm 150V 0.5% .12W 25ppm 1206
R20E
InductorRight_Pwr+
ALL COLUMNS
Primary Inductor Output Side
-2V to 85V
Place 1M R close to Spdt, place Spdt close to 8:1 mux
ACOM
4.3V_APwr
U20E
Switch: 1x SPDT, NLAST4599, 10nA +-1Vhead 5.5V, 0.8/2V, 10pF 50ohm SOT363

-2V to 85V Ampln, Gain = -0.030 = -30K/1M, AmpOut = 2.81V - (Ampln x 0.030)
85V / 1M = 85uA. 85V x 85uA = 6mW. 20nA x 1M = 20mV error
2:1 vDivider (10K ohm, 10K ohm) converts FGPA 0.4V/3.05V to 0.7V/2.02V
Dout Control from FPGA, 1 = enable
-1V_APwr
RN22A
Res4: 10Kohm 50V 5% .06W 1206vex
FPGA_EN_InductorRight_Pwr+
0.7V to 2V
RN22B
Res4: 10Kohm 50V 5% .06W 1206vex
-1V_APwr

FPGA: 0.4V to 3.1V
2:1 vDivider (10K ohm, 10K ohm)
10K x 10pF = 100nSec
Hi: (3V - -1V)/2 = 2V
Lo: (0.4V - -1V)/2 = 0.7V

Main Amplifier

2.81VDC
Main Amplifier
30K
MainAmplifier_Vin-

ALL COLUMNS HAVE THIS
NLAST, 5nA, +-1Vheadroom, Pin 9 = A, Vee pin makes Din is easy, $0.35
Mux: 8:1, NLAST4051, 5nA +-1Vhead 5.5V, 0.8/2V, 8pF 46ohm TSSOP16
U21

Y7 (4), Y6 (12), Y5 (5), Y4 (14), Y3 (2), Y2 (15), Y1 (1), Y0 (13)
OUT (3)
C (11) MuxInv_Bank1_M2
B (10) MuxInv_Bank1_M1
A (9) MuxInv_Bank1_M0
From FPGA, LVC 3.3V, 2mA
Low = On
ENABLE (6) MuxInv_Bank1_ENABLE
From FPGA, LVC 3.3V, 2mA, 0 = ON
0V when not used
V- (7) -1V -1V_APwr
GND (8) ACOM
V+ (16) 4.3V 4.3V_APwr
Provide +-1V headroom via -1V/4.3Vpwr

MuxInv_Bank2_OUTPUT_Col1
COLUMN #1 ONLY
MuxInv_Bank3_OUTPUT_Col1Row1
ONLY ROW #1, COLUMN #1

ResTF: 33Kohm 75V 0.5% .06W 25ppm 0603
R20F
Master_vCal_BUFF
-50mV to 3.05V measurement
Gain = -30K/33K
AmpOut = 2.81V - (Ampln x 0.90)
0V .. 3.1V calibration voltage
This is used to calibrate the other channels.

Title			
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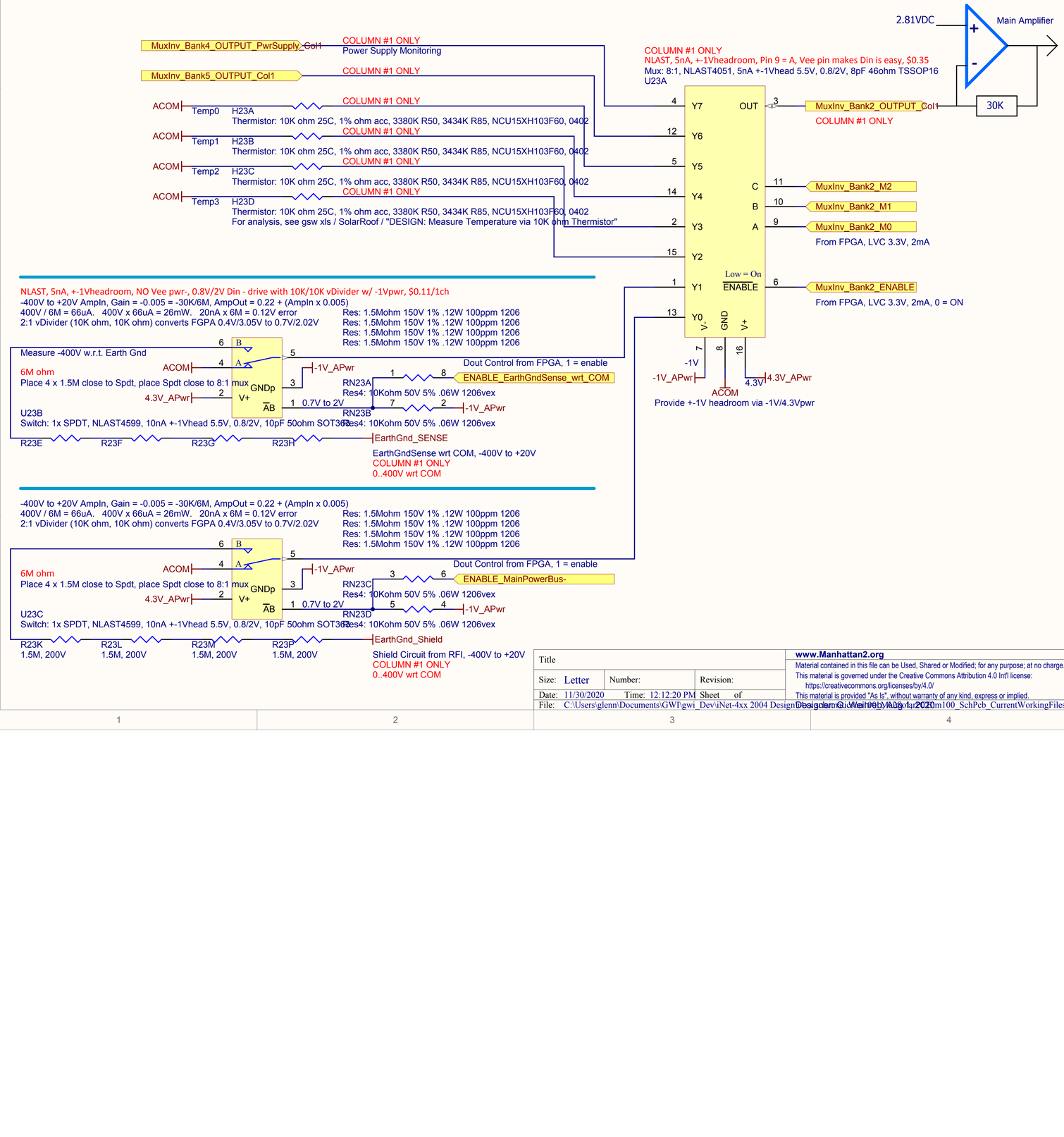
Date: 11/30/2020	Time: 12:12:20 PM	Sheet of	
File: C:\Users\glenn\Documents\GWI\gwi_Dev\iNet-4xx 2004 Design\Pcb\m100_SchPcb_CurrentWorkingFiles\Schematics\m100 Specific\m100_Mux_Inverter1.SchDoc		Designer: G. Weinreb	

MAIN MULTIPLEXOR -- BANK 2 -- Inverting Input Channels

For Mathematical Analysis, see "Amplifier_400V_SE_1MHz_Mux_Between_Rg-Rfb...TSC"
COLUMN #1 ONLY

SUMMARY
> Main Voltage Measurement
> Supports measuring high voltages
> Very precise

DESIGN FILES
> Simulation: "Amplifier_400V_SE_1MHz_Mux_Between_Rg-Rfb...TSC"
> Analysis: GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "DESIGN: Measure High Volt via Inverting Op-Amp...", "Power and Voltage Range Strategy...", "Current and Voltage Measurements", "Component Characteristics As Noted in Datasheets"
> Ma2_Solar_RD_PLAN.pdf / "Voltages are prepared for Measurement"



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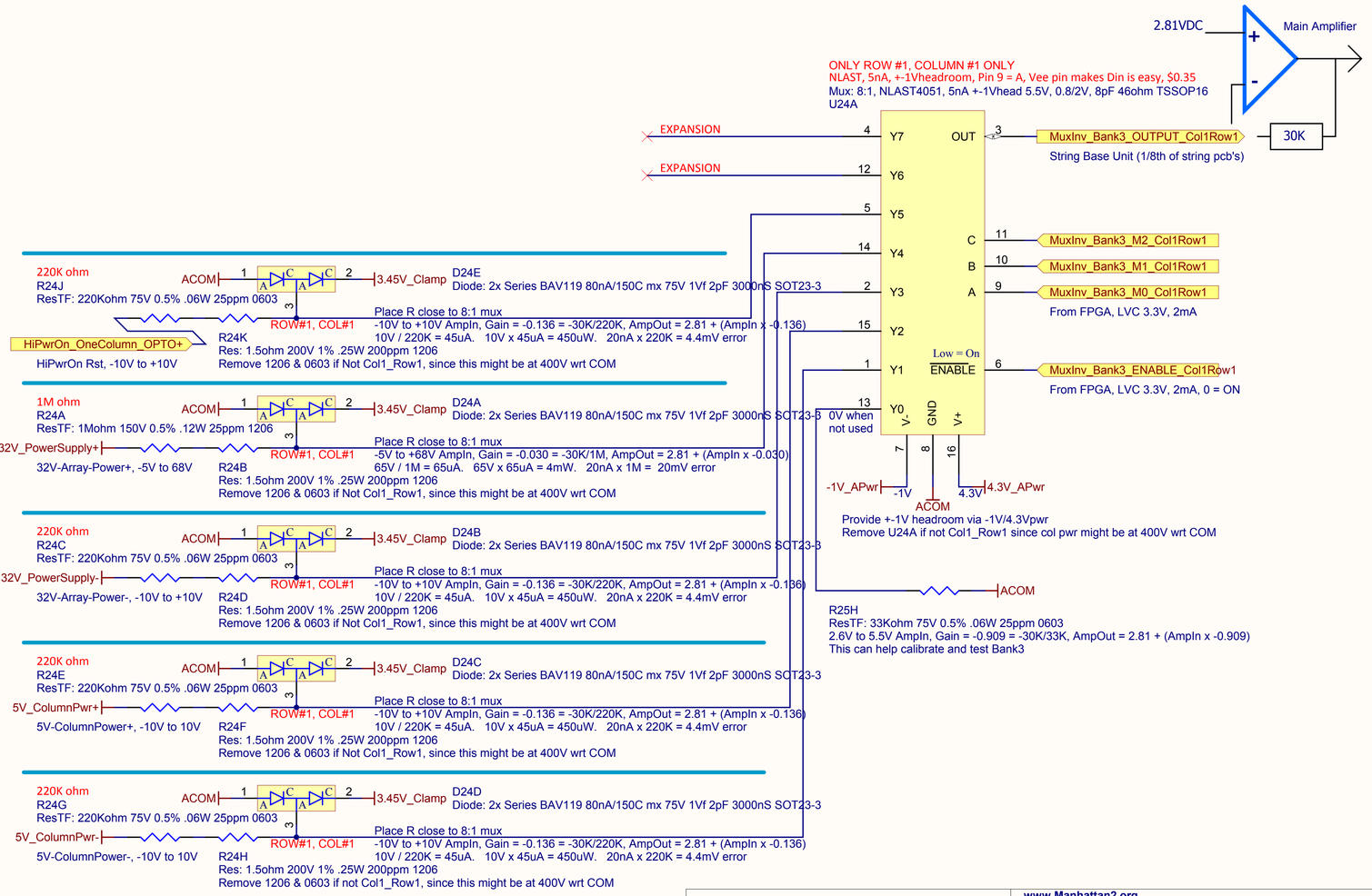
MAIN MULTIPLEXOR -- BANK 3 -- Inverting Input Channels

ONLY ROW #1, COLUMN #1 ONLY



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Date: 11/30/2020	Time: 12:12:20 PM	Sheet of	
File: C:\Users\glenn\Documents\GWI\gwi_Dev\iNet-4xx 2004 Design\Designs\m100_SchPcb_CurrentWorkingFiles\Schematics\m100 Specific\m100_Mux_Inverter3.SchDoc			

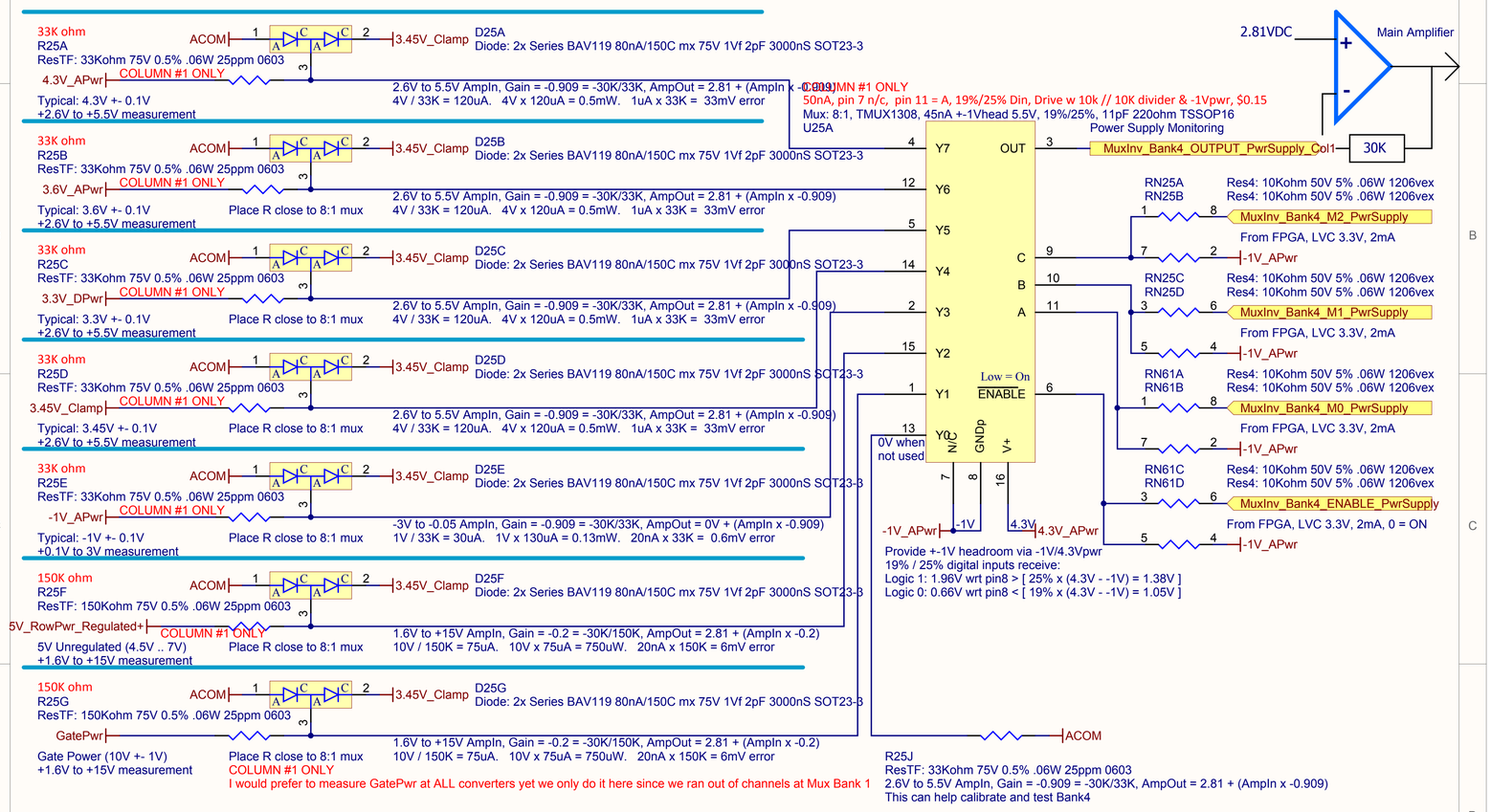
MAIN MULTIPLEXOR -- BANK 4 -- Inverting Input Channels

Power Supply Readback

COLUMN #1 ONLY

DESIGN FILES

> Simulation: "Amplifier_400V_SE_1MHz_Mux_Between_Rg-Rfb...TSC"
> Analysis: GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "DESIGN: Measure High Volt via Inverting Op-Amp...", "Power and Voltage Range Strategy...", "Current and Voltage Measurements", "Component Characteristics As Noted in Datasheets"
> Ma2_Solar_RD_PLAN.pdf / "Voltages are prepared for Measurement"



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Size: Letter	Number:	Revision:	
Date: 11/30/2020	Time: 12:12:20 PM	Sheet of	
File: C:\Users\glenn\Documents\GWI\gwi_Dev\iNet-4xx 2004 Design\Designs\m100_SchPcb_CurrentWorkingFiles\Schematics\m100 Specific\m100_Mux_Inverter4.SchDoc			

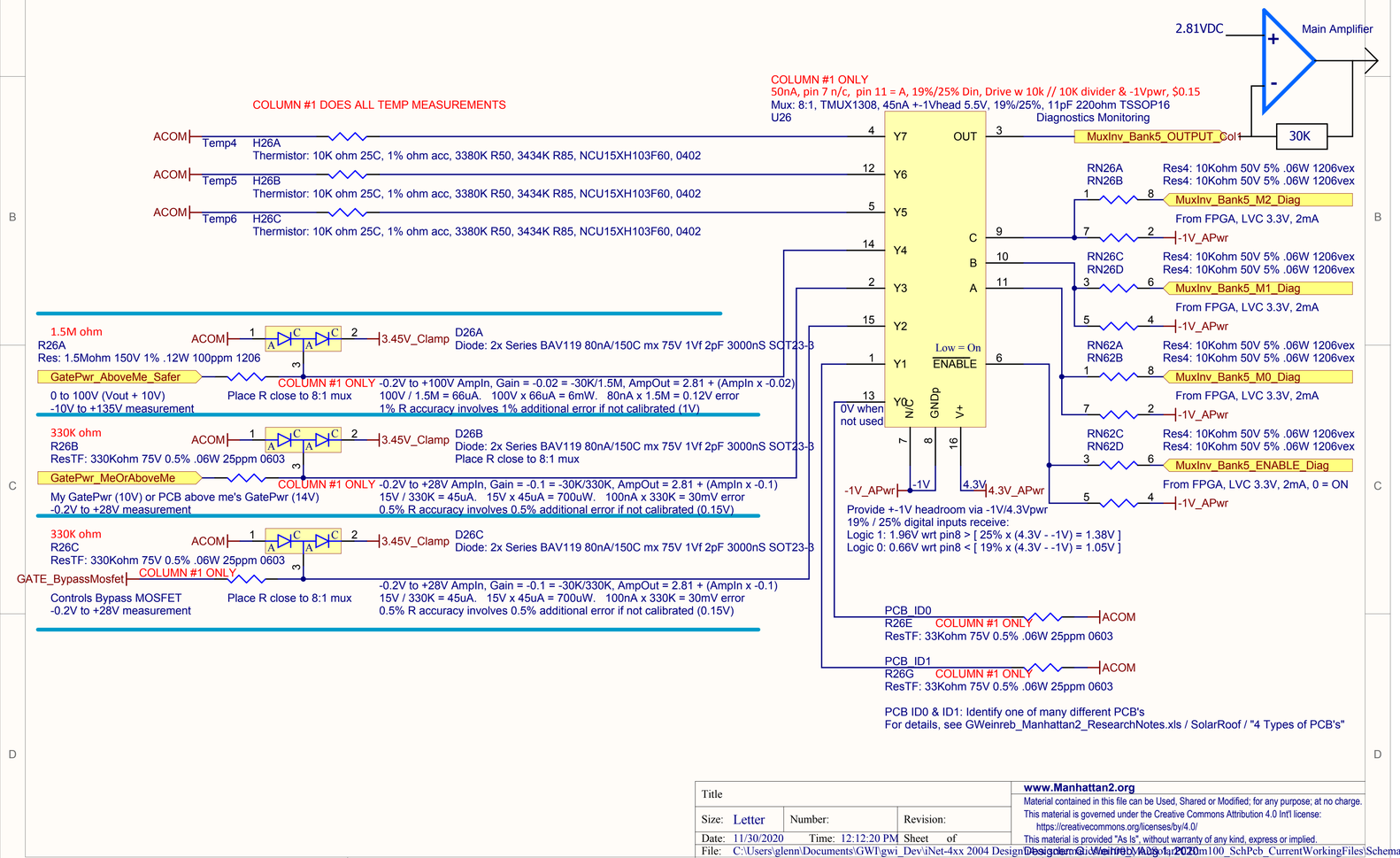
MAIN MULTIPLEXOR -- BANK 5 -- Inverting Input Channels

Diagnostics

COLUMN #1 ONLY

DESIGN FILES

> Simulation: "Amplifier_400V_SE_1MHz_Mux_Between_Rg-Rfb...TSC"
> Analysis: GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "DESIGN: Measure High Volt via Inverting Op-Amp...", "Power and Voltage Range Strategy...", "Current and Voltage Measurements", "Component Characteristics As Noted in Datasheets"
> Ma2_Solar_RD_PLAN.pdf / "Voltages are prepared for Measurement"



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Scale and Buffer High Voltages For Voltage Measurement, Detect Overvoltage (>88V), and Detect UnderVoltage (<3V)

ALL COLUMNS HAVE THIS

SUMMARY

> Scale voltage 1/30, detect overvoltage (>88V), detect undervoltage (<3V), and OpAmp buffer for Vmeasure mux.
> Digital outputs from comparator go to FPGA who can respond quickly
> Op Amp buffers drive uProcessor Ain pins and/or Mux

DESIGN FILES

> Simulation: "Detect_88V_Overvoltage_Comparator_...TSC" and "Detect_3V_Any_Voltage_Comparator...TSC"
> Analysis: GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "Things to Measure At Night with No PV Power..", Detects Voltage...", "Calibration System"
> Ma2_Solar_RD_PLAN.pdf / "Power Supply and Voltage Reference"

Scale 1/30

For mathematical analysis see: Detect_88V_Overvoltage_Comparator_...TSC

$0.013 Place close to OpAmp Input
R60A ResTF: 1Mohm 150V 0.5% .12W 25ppm 1206
PvPwr_Panel+ <100V
PV Power+ (solar panel out)
Place close to Comparator
1/(6 x 2e3 x 1e-6) = 83Hz, 2mSec TC, 10x TC = 20mSec
$0.007
ResTF: 33Kohm 75V 0.5% .06W 25ppm 0603
R60B $0.01

R60C ResTF: 1Mohm 150V 0.5% .12W 25ppm 1206
Place close to OpAmp Input
Vout_Pwr+ <100V
Primary Dc-to-Dc Converter Output
R60D
ResTF: 33Kohm 75V 0.5% .06W 25ppm 0603
R60E
ResTF: 1Mohm 150V 0.5% .12W 25ppm 1206
Place close to Input
PvPwr_Filtered+ <100V
Filter Output (after PV Input)
R60F
ResTF: 33Kohm 75V 0.5% .06W 25ppm 0603
R60G
ResTF: 1Mohm 150V 0.5% .12W 25ppm 1206
Place close to OpAmp Input
InductorLeft_Pwr+ <100V
Primary Inductor Input Side
R60H
ResTF: 33Kohm 75V 0.5% .06W 25ppm 0603
R60J
ResTF: 1Mohm 150V 0.5% .12W 25ppm 1206
Place close to OpAmp Input
InductorRight_Pwr+ <100V
Primary Inductor Output Side
R60K
ResTF: 33Kohm 75V 0.5% .06W 25ppm 0603
2.81Vref_BUFFERED_Col_N
2.81V
Do not load this w/ a capacitor
Each column has one of these.

PCOM

Detect overVoltage (>88V)

$0.14
Comparator: 4ch LMV339 OC out 9mVos 400nA OT TSSOP14
U60A
4.3V_APwr
2.81V
ToFPGA_Overvoltage_PvPwr
PV Power+ (solar panel out)
Open Collector Output (low if in+ > in-)
Connect to FPGA w/ internal pull-up
ALL COLUMNS HAVE THIS

Primary Dc-to-Dc Converter Output
Open Collector Output (low if in+ > in-)
Connect to FPGA w/ internal pull-up
ALL COLUMNS HAVE THIS
U60B
ToFPGA_Overvoltage_Vout_Pwr

Filter Output (after PV Input)
Open Collector Output (low if in+ > in-)
Connect to FPGA w/ internal pull-up
ALL COLUMNS HAVE THIS
U61A
ToFPGA_Overvoltage_FiltrOut_Pwr

Primary Inductor Input Side
Open Collector Output (low if in+ > in-)
Connect to FPGA w/ internal pull-up
ALL COLUMNS HAVE THIS
U61B
ToFPGA_Overvoltage_InductorLeft_Pwr

Primary Inductor Output Side
Open Collector Output (low if in+ > in-)
Connect to FPGA w/ internal pull-up
ALL COLUMNS HAVE THIS
U61C
ToFPGA_Overvoltage_InductorRight_Pwr

Detect UNDER voltage (<3V)

For mathematical analysis see: Detect_3V_Any_Voltage_Comparator...TSC

$0.14
Comparator: 4ch LMV339 OC out 9mVos 400nA OT TSSOP14
U60C
94mVref_Unbuffered
94mV
ToFPGA_UNDERvoltage_PvPwr
PV Power+ (solar panel out)
Open Collector Output (low if in+ > in-)
Connect to FPGA w/ internal pull-up

C60B
Cap: 1uF 16V 20% 125C 0603
Place close to Comparator
1/(6 x 2e3 x 1e-6) = 83Hz, 2mSec TC, 10x TC = 20mSec

Comparator: 4ch LMV339 OC out 9mVos 400nA OT TSSOP14
U60D
94mV
ToFPGA_UNDERvoltage_Vout_Pwr
Primary Dc-to-Dc Converter Output
Open Collector Output (low if in+ > in-)
Connect to FPGA w/ internal pull-up

LMV339, 4x, OC out, 9mVos, 400nA OT, -0.1 to Vcc-1, 0.4uSec/100mV, 5Vcc, $0.14/4ch, 87uA/ch, Arrow ST #LMV339IPT Tssop14 is $0.14

ANALYSIS

Gain = 33/(33+1000) = 0.0319 = 1 / 31.3

+- 400nA leakage x 33K = +-13mV at comparator Input 13mVos x 31 = 400mV error wrt Vin, 0.4/88 = 0.5%. One can see this error via simulator.

1M and 33K are accurate to 0.5%, and this gives you 1% accuracy. You can calibrate this out with 16bit a/d that reads same thing.

88Vin / 31.3 Gain = 2.811V

100V / 1MEG = 100uA, 10mW
50V / 1MEG = 50uA, 2.5mW

Delay observed on sim w/ 0 to 90V Square Wave: 400nSec

9mVos x 31 = 300mV error wrt Vin, 0.3/88 = 0.3%

threshold vRef accuracy = 0.5% (Rt) + %0.5% (Rb) + 0.2% ref = 1.2%

Accuracy wrt Vin and 88V threshold
= 1% (R1) + 0.5% (R2) + 0.5% (leakage) + 0.3% (Vos) + 1.2% (vRef)
= (1+.5+.5+.3+1.2) = +- 3.5%, 3.5% x 88 = +-3V

FPGA Detects Analog Pwr

R60L
Res: 3.9Kohm 75V 1% .06W 100ppm 0603
3.6V/4K = 1mA if APwr on and DPwr off
3.6V_APwr
ToFPGA_3.6V_APwr_GOOD
3.6V+-0.1V
hi if analog pwr is good
Connect to FPGA w/ internal pull-DOWN

NOTE: GatePwr is detected via PGOOD at GatePwr vReg

Op Amp Buffer

For simulation, see "100Vmeasure - vDivider to Op Amp, v1a.TSC"
CALIBRATION: measure here and also via main amp inverter

OpAmp: TLV9064 4ch 10MHz 2mVos 25pA 80dB 750uA-ch TSSOP14
U62A
3.6V_APwr
PvPwr_BUFF
To Vmeasure Mux
ACOM

OpAmp: TLV9064 4ch 10MHz 2mVos 25pA 80dB 750uA-ch TSSOP14
U62B
TLV906x, 10MHz, 0.2uS Rec, 2mVos max OT, 4pF, 25pA typ 85C, 6V/uS, 80dB min OT, In -0.1 to (Vcc-1.4), Out 0.15V to (Vcc-0.15V), 750uA/ch, $0.49
Vout_Pwr_BUFF
To Vmeasure Mux

OP AMP BUFFER
> OpAmp 0V/3.6V power supply means we can drive uProcessor w/o damage due to overvoltage since uProcessor is also powered by 3.6V.
> op amp input range is -0.1V to (3.6V-1.4V) = 2.4V (i.e. 3.6V pwr, 1.4V +Headroom)
> 2.4V x (1e6 + 33e3) / 33e3 = 75V max vin for analog measurement
> Simulator sees 1.3MHz bw

OpAmp: TLV9064 4ch 10MHz 2mVos 25pA 80dB 750uA-ch TSSOP14
U62C
InductorLeft_Pwr_BUFF
To Vmeasure Mux

OpAmp: TLV9064 4ch 10MHz 2mVos 25pA 80dB 750uA-ch TSSOP14
U62D
InductorRight_Pwr_BUFF
To Vmeasure Mux

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Power Conversion, Buck Converter

For simulation, see "Gate_Drv_Testing_UCC27282_2xFet_Switch_v14f.TSC"
For analysis, see GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "Buck Converter Math"
ALL COLUMNS HAVE THIS

PvPwr_Filtered+

Left_Hi MOSFET
MOSFET: N-ch DMT10H009 100V 8mOhm PowerTDFN8
M30A
GATE_Left_Hi

Left_Lo MOSFET
MOSFET: N-ch DMT10H009 100V 8mOhm PowerTDFN8
M30B
GATE_Left_Lo

vMeas_Shunt3_Buck+
Shunt3, Measure Buck Current
8A x 0.001 ohm = 8mV, 64mW
Res: 1mOhm 5% 3W 54A 75ppm 2512
R30A
vMeas_Shunt3_Buck-

PCOM
This R gives PCB trace unique netname
RN34A Res4: 2.2ohm 50V 5% .06W 1206vex
RN34B Res4: 2.2ohm 50V 5% .06W 1206vex

InductorLeft_Pwr+
L30 Ind: 56uH 4A 56mOhm 13x12x7mm
L31 Ind: 56uH 4A 56mOhm 13x12x7mm
L32 Ind: 56uH 4A 56mOhm 13x12x7mm
L33 Ind: 56uH 4A 56mOhm 13x12x7mm

#HCM1A1307V2-560-R, 4 x $0.85 = $3.40
4 in parallel, 56mH/4 = 14mH, 56mOhm/4 =14m ohm
8A x 14mOhm = 100mV, 800mW

L_Left
TP30A

Power Conversion, Boost Converter

InductorRight_Pwr+

R_Right
TP30B

Right_Hi MOSFET
MOSFET: N-ch DMT10H009 100V 8mOhm PowerTDFN8
M31A
GATE_Right_Hi

Right_Lo MOSFET
MOSFET: N-ch DMT10H009 100V 8mOhm PowerTDFN8
M31B
GATE_Right_Lo

vMeas_Shunt4_Boost+
Shunt4, Measure Boost Current
8A x 0.001 ohm = 8mV, 64mW
Res: 1mOhm 5% 3W 54A 75ppm 2512
R31A
vMeas_Shunt4_Boost-

These R's give PCB trace unique netname
RN31C Res4: 2.2ohm 50V 5% .06W 1206vex
RN31D Res4: 2.2ohm 50V 5% .06W 1206vex

Output Capacitor

Vout
TP31C

C_out
TP31B

C32A Cap: 2.2uF 100V 20% 125C 1210
C32B Cap: 2.2uF 100V 20% 125C 1210
C32C Cap: 2.2uF 100V 20% 125C 1210
C32D Cap: 2.2uF 100V 20% 125C 1210
C32E Cap: 2.2uF 100V 20% 125C 1210
C32F Cap: 2.2uF 100V 20% 125C 1210
C32G Cap: 2.2uF 100V 20% 125C 1210
C32H Cap: 2.2uF 100V 20% 125C 1210
C32J Cap: 2.2uF 100V 20% 125C 1210
C32K Cap: 2.2uF 100V 20% 125C 1210
C32L Cap: 2.2uF 100V 20% 125C 1210
C32M Cap: 2.2uF 100V 20% 125C 1210

Vsource: C_out on right, I_source: C_out on left or L, is this ok w/ BOOST converter?

PwrOut-

vMeas_Shunt5_Cout-
Shunt5, Measure Cout Current
8A x 0.001 ohm = 8mV, 64mW
Res: 1mOhm 5% 3W 54A 75ppm 2512
R33C
vMeas_Shunt5_Cout+

RN32A Res4: 2.2ohm 50V 5% .06W 1206vex
RN32B Res4: 2.2ohm 50V 5% .06W 1206vex
These R's give PCB trace unique netname

Bypass Mosfet

ElementTop
TP33A
4-40 bolt/standoff
Vout_Pwr+

M33A
MOSFET: N-ch TPH3R70A 100V 4mOhm 8-SOP-Advance
Bypass Mosfet (bypass entire DC-DC converter if it fails)
TPH3R70APL1Q, N-Chan, $0.61, 8-PowerVDFN, 100V, 4 m ohm, 2.5Vgs th

GATE_BypassMosfet
Controls Bypass MOSFET, which shorts element
Top to Bottom when DC-to-DC is OFF.

Z33
Zener: 13Vz 5% C .2W 100pF SOT23-3

ALL COLUMNS HAVE THIS
Bypass MOSFET
Shorts string Top to Bottom. Only engaged when
this DC-to-DC converter is being bypassed --
when occurs when this is OFF for some reason.

vMeas_Shunt6_BypassMosfet+
Shunt6, Measure Bypass Mosfet Current
8A x 0.001 ohm = 8mV, 64mW
Res: 1mOhm 5% 3W 54A 75ppm 2512
R33A
vMeas_Shunt6_BypassMosfet-

This R gives PCB trace unique netname
RN33A Res4: 2.2ohm 50V 5% .06W 1206vex
RN33B Res4: 2.2ohm 50V 5% .06W 1206vex

PLACE SHUNTS 7 & 8 NEXT TO EACH OTHER

vMeas_Shunt7_String+
Shunt7 Measure String Current
8A x 0.001 ohm = 8mV, 64mW
Res: 1mOhm 5% 3W 54A 75ppm 2512
R33B
vMeas_Shunt7_String-

These R's give PCB trace unique netname
RN33C Res4: 2.2ohm 50V 5% .06W 1206vex
RN33D Res4: 2.2ohm 50V 5% .06W 1206vex

ElementBottom
TP33B
4-40 bolt/standoff
ElementBottom

PV Power Filter

For simulation, see "Gate_Drv_Testing_UCC27282_2xFet_Switch_v14f.TSC"
For simulation, see GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "DC-to-DC Converter Input filter..."

TP34A
4-40 bolt/standoff
PvPwr_Panel+

PvPwr_Panel+
ALL COLUMNS HAVE THIS

C34A Cap: 2.2uF 100V 20% 125C 1210
C34B Cap: 2.2uF 100V 20% 125C 1210
C34C Cap: 2.2uF 100V 20% 125C 1210
C34D Cap: 2.2uF 100V 20% 125C 1210

L34
Ind: 1.3uH 18A 2.3mOhm 12x10x6mm

C35A Cap: 2.2uF 100V 20% 125C 1210
C35B Cap: 2.2uF 100V 20% 125C 1210
C35C Cap: 2.2uF 100V 20% 125C 1210
C35D Cap: 2.2uF 100V 20% 125C 1210
C35E Cap: 2.2uF 100V 20% 125C 1210

R35
Res: 330mOhm 5% 1W 400ppm 2512

Power Input Capacitor (Cin)

C36A Cap: 2.2uF 100V 20% 125C 1210
C36B Cap: 2.2uF 100V 20% 125C 1210
C36C Cap: 2.2uF 100V 20% 125C 1210
C36D Cap: 2.2uF 100V 20% 125C 1210
C36E Cap: 2.2uF 100V 20% 125C 1210
C36F Cap: 2.2uF 100V 20% 125C 1210
C36G Cap: 2.2uF 100V 20% 125C 1210
C36H Cap: 2.2uF 100V 20% 125C 1210
C36J Cap: 2.2uF 100V 20% 125C 1210
C36K Cap: 2.2uF 100V 20% 125C 1210

PvPwr_Filtered+
PvPwr_Filtered+
Test Point for Monitoring and Testing
4-40 bolt/standoff
TP35A

PCOM
Test Point for Monitoring and Testing
4-40 bolt/standoff
TP35B

PV Panel
25V .. 75V

PvPwr_Panel-
TP34B
4-40 bolt/standoff

PvPwr_Panel-
ALL COLUMNS HAVE THIS

Shunt2, Measure PV Filter Current
8A x 0.001 ohm = 8mV, 64mW

PLACE SHUNTS 1 & 2 NEXT TO EACH OTHER

vMeas_Shunt2_PvPwr-
Shunt2, Measure PV Current
8A x 0.001 ohm = 8mV, 64mW
Res: 1mOhm 5% 3W 54A 75ppm 2512
R36A
vMeas_Shunt2_PvPwr+

RN36C Res4: 2.2ohm 50V 5% .06W 1206vex
RN36D Res4: 2.2ohm 50V 5% .06W 1206vex
These R's give PCB trace unique netname

vMeas_Shunt1_InputPwr-
Shunt1, Measure Input Current
8A x 0.001 ohm = 8mV, 64mW
Res: 1mOhm 5% 3W 54A 75ppm 2512
R36B
vMeas_Shunt1_InputPwr+

RN36A Res4: 2.2ohm 50V 5% .06W 1206vex
RN36B Res4: 2.2ohm 50V 5% .06W 1206vex
These R's give PCB trace unique netname

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Designed by: Weinreb, Aug 5, 2020

i60x instruNet Schematics

m100_Group_AtoD_and_Calibration.SchDoc
m100_Group_AtoD_and_Calibration.SchDoc

m100_Group_Measurement.SchDoc
m100_Group_Measurement.SchDoc

m100_Group_Power_Conversion.SchDoc
m100_Group_Power_Conversion.SchDoc

m100_Group_Communication.SchDoc
m100_Group_Communication.SchDoc

m100_Group_Power_Supply.SchDoc
m100_Group_Power_Supply.SchDoc

m100_Group_System.SchDoc
m100_Group_System.SchDoc

m100_Group_Array.SchDoc
m100_Group_Array.SchDoc

Fiducias

FD10
z NoPART: FIDUCIA-1mm-3mm
Permitted Layers Rule [Permitted Layers - Top,]

FD11
z NoPART: FIDUCIA-1mm-3mm
Permitted Layers Rule [Permitted Layers - Top,]

FD12
z NoPART: FIDUCIA-1mm-3mm
Permitted Layers Rule [Permitted Layers - Top,]

FD20
z NoPART: FIDUCIA-1mm-3mm
Permitted Layers Rule [Permitted Layers - Bottom]

FD21
z NoPART: FIDUCIA-1mm-3mm
Permitted Layers Rule [Permitted Layers - Bottom]

FD22
z NoPART: FIDUCIA-1mm-3mm
Permitted Layers Rule [Permitted Layers - Bottom]

PCB Registration Holes

RH1
0.128" dia pcb assm/test registration hole
z NoPART: 0.128in registration hole
Permitted Layers Rule [Permitted Layers - Top,]

RH2
0.128" dia pcb assm/test registration hole
z NoPART: 0.128in registration hole
Permitted Layers Rule [Permitted Layers - Bottom]

m100 Pcb

RAW PCB

PCB: m100
P1

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Communication Between Adjacent Array Elements within One Row

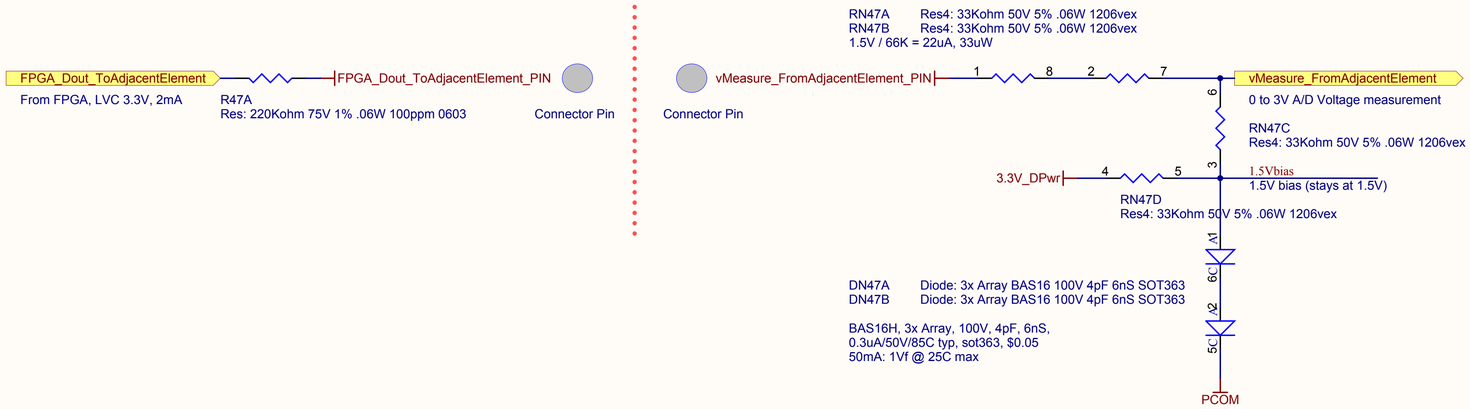
> Adjacent converters communicate before receiving CANbus address to help determine address during discovery phase.
ALL COLUMNS HAVE THIS

DESIGN FILES
> Simulation: "Comm_Between_Array_Base_Elements_v2.TSC"
> Analysis: GWeinreb_Manhattan2_ResearchNotes.xls / SolarRoof / "Communication Bet Adjacent Elements"

SIGNALLING BETWEEN ARRAY BASES (e.g. string 0 element 0 to string 1 element 0).

Assume +-5V common mode voltage between GND's of adjacent BASES. Parts: 200K ($0.002), 4Res netwc ($0.01), Diode Array ($0.04), Mux Ch ($0.03) = $0.08 total

Dout	CMV	Amp_Out
0.5V	+5V	1.63 V
2.8V	+5V	1.86 V
0.5V	-5V	.63 V
2.8V	-5V	.86 V
0.5V	0V	1.13 V
2.8V	0V	1.36 V



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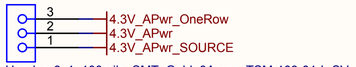
Designed: Weinreb Aug 25, 2020

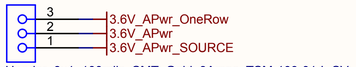
Row Connectors -- Connect together Multiple PCB's on one Row

ALL COLUMNS HAVE THIS

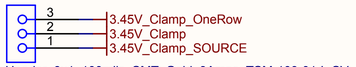
Column #1 PCB supplies entire Row w/ power



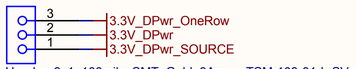
Header, 3x1, 100mils, SMT, Gold, 3Amps, TSM-103-01-L-SV
J20



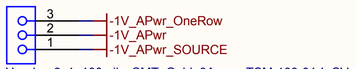
Header, 3x1, 100mils, SMT, Gold, 3Amps, TSM-103-01-L-SV
J2



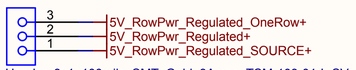
Header, 3x1, 100mils, SMT, Gold, 3Amps, TSM-103-01-L-SV
J3



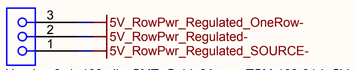
Header, 3x1, 100mils, SMT, Gold, 3Amps, TSM-103-01-L-SV
J4



Header, 3x1, 100mils, SMT, Gold, 3Amps, TSM-103-01-L-SV
J5



Header, 3x1, 100mils, SMT, Gold, 3Amps, TSM-103-01-L-SV
J6



Header, 3x1, 100mils, SMT, Gold, 3Amps, TSM-103-01-L-SV
J7

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File: C:\Users\glenn\Documents\GWI\gwi_Dev\iNet-4xx 2004 Design\Schematics\m100 Specific\m100_Row_Connectors.SchDoc		Designed by: Glenn Weinreb, Aug 25, 2020	

Xmc4200 Microcontroller ADC

ALL COLUMNS HAVE THIS

Platform To Go: https://www.infineon.com/dgdl/Infineon-XMC4200_Platform2Go-UserManual-v01_00-EN.pdf?fileId=5546d4626f229553016f8fca76c12c96
Platform To Go: https://www.infineon.com/dgdl/Infineon-XMC4200_Platform2Go-UserManual-v01_00-EN.pdf?fileId=5546d4626f229553016f8fca76c12c96

Two A/D's Process Each Conversion Cycle in Real-time

Measure_7x_CurrentShunts_1.5MHz_BW
0 to 3.3V measurement, 1.5MHz BW
0 to 3V, 115mV/Amp with 1m ohm shunt

A/D input is dynamic load and RC helps to stabilize it
R19E
Res: 220ohm 75V 1% .06W 100ppm 0603
200nA leakage x 200 ohms = 40uV error
C19E
Cap: 100pF 100V 5% npo 125C 0603
100pF x 200ohms = 20nSec
ACOM

Measure_Vout_5MHz_BW
0 to 3.3V measurement

A/D input is dynamic load and RC helps to stabilize it
R19D
Res: 220ohm 75V 1% .06W 100ppm 0603
200nA leakage x 200 ohms = 40uV error
C19D
Cap: 100pF 100V 5% npo 125C 0603
100pF x 200ohms = 20nSec
ACOM

Calibration Occurs when DC-to-DC is not running (and try to do some measurements inbetween DC-to-DC cycles)

?? what is our strategy for a/d measurements during dc-to-dc conversion? only col1 has 16bit a/d. can we slip alternative channel inbetween cycles? should all colums have 16bit a/d?
If we are doing voltage regulation we could slip in diagnostic voltage measurement every N cycles of current measurement.
If we are doing current regulation we could slip in diagnostic voltage measurement every N cycles of voltage measurement.

Master_vCal_BUFF
0 to 3.3V measurement

A/D input is dynamic load and RC helps to stabilize it
R19C
Res: 220ohm 75V 1% .06W 100ppm 0603
200nA leakage x 200 ohms = 40uV error
C19C
Cap: 100pF 100V 5% npo 125C 0603
100pF x 200ohms = 20nSec
ACOM

MainAmplifier_Vout
0 to 3.3V measurement

A/D input is dynamic load and RC helps to stabilize it
R19A
Res: 220ohm 75V 1% .06W 100ppm 0603
200nA leakage x 200 ohms = 40uV error
C19A
Cap: 100pF 100V 5% npo 125C 0603
100pF x 200ohms = 20nSec
(100e-12 * 200 * 6.28)^-1 = 8MHz
ACOM

PvPwr_BUFF
PvPwr, Buffered, G=0.0319
0 to 3.3V measurement

A/D input is dynamic load and RC helps to stabilize it
R19F
Res: 220ohm 75V 1% .06W 100ppm 0603
200nA leakage x 200 ohms = 40uV error
C19F
Cap: 100pF 100V 5% npo 125C 0603
100pF x 200ohms = 20nSec
ACOM

Vout_Pwr_BUFF
Vout, Buffered, G=0.0319
0 to 3.3V measurement

A/D input is dynamic load and RC helps to stabilize it
R19B
Res: 220ohm 75V 1% .06W 100ppm 0603
200nA leakage x 200 ohms = 40uV error
C19B
Cap: 100pF 100V 5% npo 125C 0603
100pF x 200ohms = 20nSec
ACOM

Xmc4200 Microcontroller, Dual 12bit 5Ms/sec A/D's
3V / 12bit = 0.8mV LSB

U1E
uProc: XMC4200F64K256BAXQ, M4, 256K flash, 40k ram, LQFP-64

3.3V
20 P14.0 AIN_G0_CH0
19 P14.3 CAN_Node_0_RX
18 P14.4 AIN_G0_CH4
17 P14.5 AIN_G0_CH5
16 P14.6 AIN_G0_CH6
15 P14.7 AIN_G0_CH7
3.3V
24 P14.8 AIN_G1_CH0, DAC0
23 P14.9 AIN_G1_CH1, DAC1
14 P14.14 AIN_G1_CH6

CAN_Node_0_Receive
ToFPGA_CANBus_ArrayRow_Receive
To Fpga, 3.3V logic
1 = recessive (logic 1, termination has 0V across canbus wires)

Xmc Alternate VAREF (alternate analog ref input)
This drives Ch0 of Group#0 and Ch0 of Group#1

3.3Vref_Buff_A_Col_N
Each column has one of these.

3.3Vref drives uProcessor a/d Ref Input Pin (dynamic Load, changes w/ time)
3.3V +- 10mV Place cap close to uP IC
3.3V
C19G Cap: 10uF 10V 20% 125C 0805
C19H Cap: 10uF 10V 20% 125C 0805
0V
C19J Cap: 0.1uF 25V 20% 125C 0603
ACOM

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Xmc4200 Microcontroller

ALL COLUMNS HAVE THIS

U1D
uProc: XMC4200F64K256BAXQ, M4, 256K flash, 40k ram, LQFP-64

SPI, 16bit a/d, CS	52	P1.0	*SPI_U0C0_SELO0_CS0
SPI, 16bit a/d, SCLK	51	P1.1	*SPI_U0C0_SCLK
uP_P1.2 FPGA Interface	50	P1.2	
CCU40_OUT0 16bit_ADC_MCLK	49	P1.3	
CAN_Node_1_Receive	48	P1.4	CAN_Node_1_RX
SPI, 16bit a/d, MISO	47	P1.5	*SPI_U0C0_MISO / MRST
SPI, 16bit a/d, MOSI	55	P1.7	*SPI_U0C0_MOSI / MTSR
SPI_FPGA_Interface_SCLK	54	P1.8	SPI_U1C1_SCLK
SPI_FPGA_Interface_MOSI	53	P1.9	SPI_U1C1_MOSI / MTSR
uP_P1.5 FPGA Interface	46	P1.15	
uP_P3.0 FPGA Interface	5	P3.0	

* serial interface to 16bit a/d

U1C
uProc: XMC4200F64K256BAXQ, M4, 256K flash, 40k ram, LQFP-64

SPI_FPGA_Interface_MISO	2	P0.0	SPI_U1C1_MISO / MRST
uP_P0.1 FPGA Interface	1	P0.1	
SPI_FPGA_Interface_CS1	64	P0.2	SPI_U1C1_SELO1_CS1
uP_P0.3 FPGA Interface	63	P0.3	
uP_P0.4 FPGA Interface	62	P0.4	
uP_P0.5 FPGA Interface	61	P0.5	
uP_P0.6 FPGA Interface	60	P0.6	
TDI FPGA Interface	58	P0.7	JTAG DEBUG TDI
uP_P0.8 FPGA Interface	57	P0.8	
SPI_FPGA_Interface_CS0	4	P0.9	SPI_U1C1_SELO0_CS0
uP_P0.10 FPGA Interface	3	P0.10	
uP_P0.11 FPGA Interface	59	P0.11	
CAN_Node_0_Transmit	34	P2.0	CAN_Node_0_TX
TDO	33	P2.1	JTAG DEBUG TDO
ADC_EMUX_00	32	P2.2	ADC_EMUX_00
ADC_EMUX_01	31	P2.3	ADC_EMUX_01
ADC_EMUX_02	30	P2.4	ADC_EMUX_02
uP_P2.5 FPGA Interface	29	P2.5	
uP_P2.6 FPGA Interface	36	P2.6	
CAN_Node_1_Transmit	35	P2.7	CAN_Node_1_TX
uP_P2.8 FPGA Interface	28	P2.8	
	27	P2.9	
ADC_EMUX_11	26	P2.14	ADC_EMUX_11
ADC_EMUX_12	25	P2.15	ADC_EMUX_12

m100_16bit_AtoD.SchDoc COLUMN #1 ONLY

- ToFPGA_AtoD_SDO
- FPGA_AtoD_SCK
- FPGA_AtoD_SDI
- FPGA_AtoD_CS
- ToFrom_FPGA_AtoD_MCLKIN — CCU40_OUT0
- ToFPGA_AtoD_IRQ_MDAT

FPGA, LVC 3.3V, 2mA

m100_CANbus_Isolated.SchDoc COLUMN #1 ONLY

- FPGA_CANBus_ArrayColumn_Transmit

From Fpga, 3.3V logic, 4mA
If uProcessor or FPGA does not boot we want this to be at 3.3V
1 = recessive (logic 1, termination puts 0V across canbus wires)
0 = dominant (logic 0, drive 2V across canbus wires)

- ToFPGA_CANBus_ArrayColumn_Receive

To Fpga, 3.3V logic
1 = recessive (logic 1, termination has 0V across canbus wires)
0 = dominant (logic 0, somone is driving 2V across canbus wires)

m100_CANbus_NotIsolated.SchDoc ALL COLUMNS HAVE THIS

- FPGA_CANBus_ArrayRow_Transmit

From Fpga, 3.3V logic, 4mA
If uProcessor or FPGA does not boot we want this to be at 3.3V
1 = recessive (logic 1, termination puts 0V across canbus wires)
0 = dominant (logic 0, drive 2V across canbus wires)

- ToFPGA_CANBus_ArrayRow_Receive — ToFPGA_CANBus_ArrayRow_Receive

To Fpga, 3.3V logic
1 = recessive (logic 1, termination has 0V across canbus wires)

- FPGA_CANBus_ArrayRow_S_Ctrl

From Fpga, 3.3V logic, 4mA
0 = transmitter enabled, 1 = receive only

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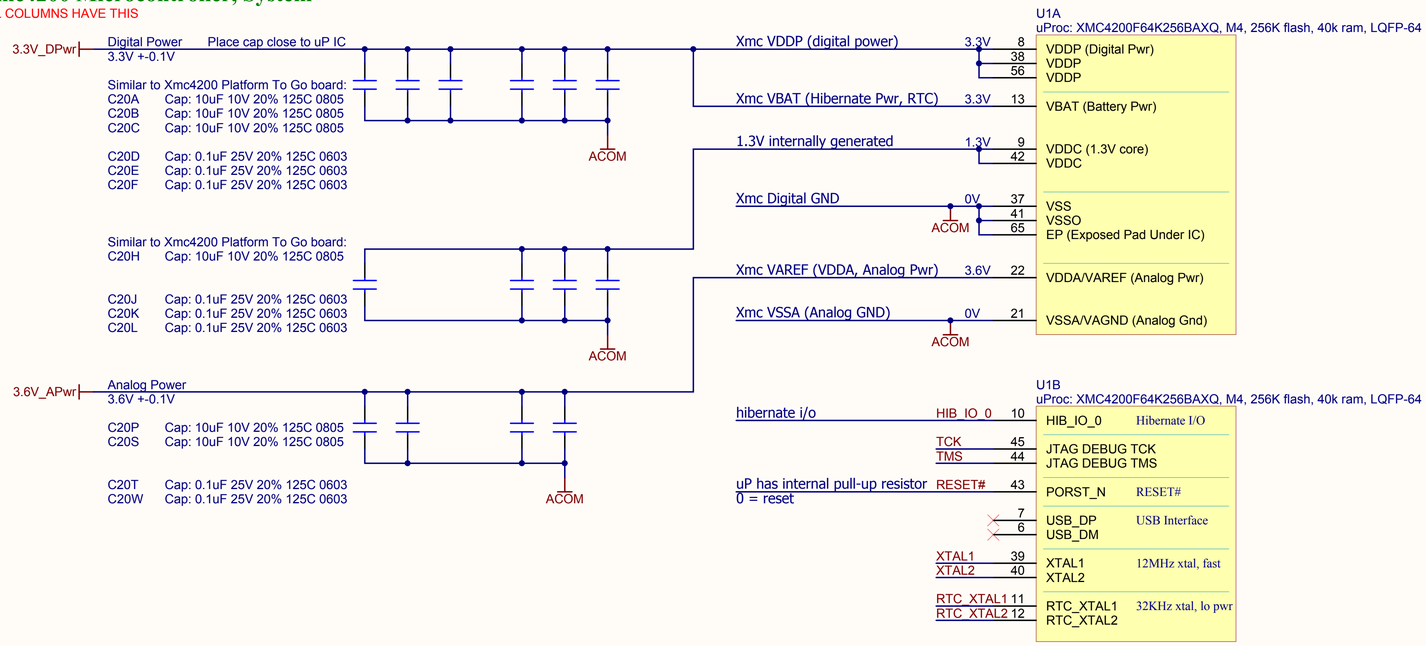
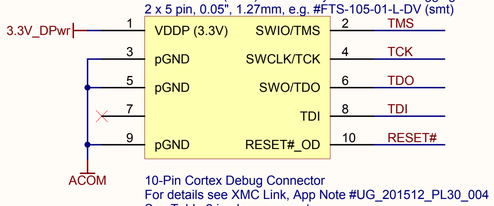
Xmc4200 Microcontroller, System

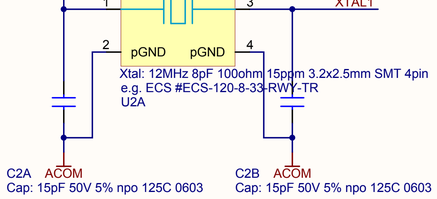
ALL COLUMNS HAVE THIS



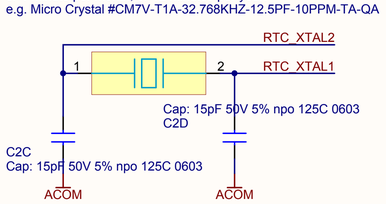
Microcontroller, 10-pin Debug Connector



Clock (12MHz, fast, more power)



RTC (32KHz, slow, low power)



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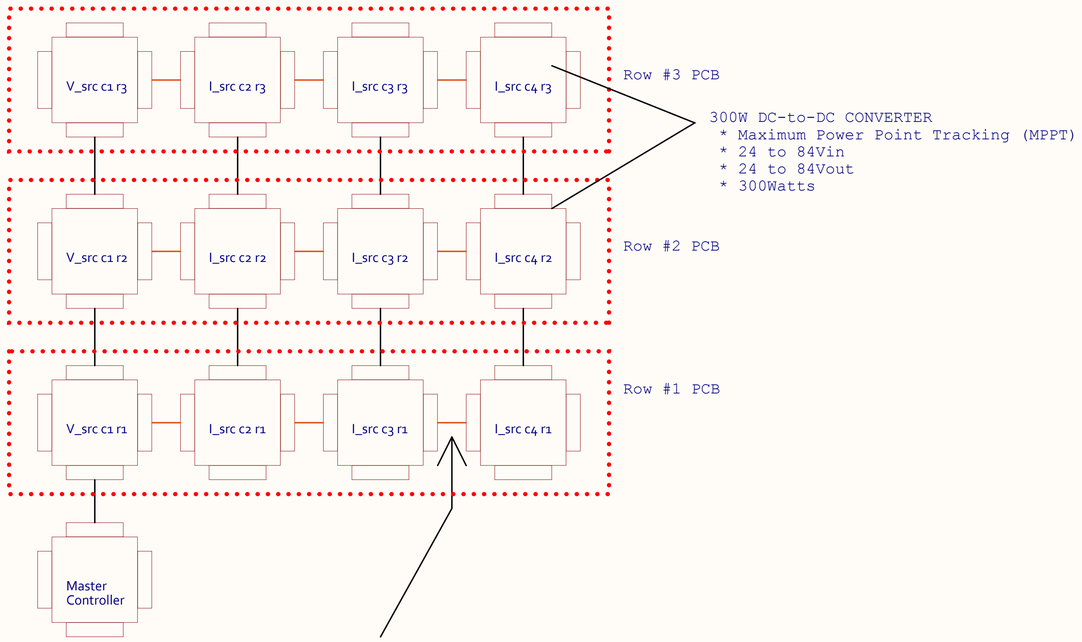
Array Connectors

m100_Row_Connectors.SchDoc
m100_Row_Connectors.SchDoc

m100_Column_Connectors.SchDoc
m100_Column_Connectors.SchDoc

Array Design



Row #3 PCB

300W DC-to-DC CONVERTER
 * Maximum Power Point Tracking (MPPT)
 * 24 to 84Vin
 * 24 to 84Vout
 * 300Watts

Row #2 PCB

Row #1 PCB

SIGNALS IN COLUMN TOP/BOTTOM CONNECTORS
 * Vout_Pwr+ (ElementTop)
 * ElementBottom
 * EarthGnd_SENSE (no current flow, GFP)
 * EarthGnd_Shield (shield RFI)
 * CAN_HI_ArrayColumn_wrt_EarthGnd (isolated, column #1 only)
 * CAN_LO_ArrayColumn_wrt_EarthGnd
 * HiPwrOn_OneColumn_OPTO+ (isolated, column #1 only)
 * 5V_ColumnPwr+ (powers isolated CANbus_OneColumn and HiPwrOn rst)
 * 5V_ColumnPwr-
 * 32V_PowerSupply+ (routes to column #1 only,
    provides power for row, 10Watt/Row, 8 rows = 80watts/3A)
 * 32V_PowerSupply-

SIGNALS IN ROW LEFT/RIGHT CONNECTORS
 * CAN_HI_OneArrayRow_wrt_COM (connects uP on 1x row)
 * CAN_LO_OneArrayRow_wrt_COM
 * FPGA_HiPwrOn_OneArrayRow_TRANSMIT
 * FPGA_HiPwrOn_OneArrayRow_RECEIVE
 * 4.3V_APwr
 * 3.6V_APwr
 * 3.3V_DPwr
 * 3.45V_Clamp
 * AGND
 * -1V_Apwr
 * 5V_RowPwr_Regulated_OneRow+
 * 5V_RowPwr_Regulated_OneRow-
 * Vout_Pwr+ (ElementTop)
 * ElementBottom

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A/D and Calibration

m100_16bit_AtoD.SchDoc
m100_16bit_AtoD.SchDoc

m100_Calibration_System.SchDoc
m100_Calibration_System.SchDoc

m100_Buffered_Vref.SchDoc
m100_Buffered_Vref.SchDoc

m100_Calibration_Voltages.SchDoc
m100_Calibration_Voltages.SchDoc

m100_3.3Vreference.SchDoc
m100_3.3Vreference.SchDoc

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Communication

m100_HiPwrOn_Source.SchDoc
m100_HiPwrOn_Source.SchDoc

m100_HiPwrOn_TmitAndRcv.SchDoc
m100_HiPwrOn_TmitAndRcv.SchDoc

m100_Row_Communication.SchDoc
m100_Row_Communication.SchDoc

m100_CANbus_Isolated.SchDoc
m100_CANbus_Isolated.SchDoc

m100_CANbus_NotIsolated.SchDoc
m100_CANbus_NotIsolated.SchDoc

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Measurement

m100_MainMeas_Amplifier.SchDoc
m100_MainMeas_Amplifier.SchDoc

m100_Current_Measurement.SchDoc
m100_Current_Measurement.SchDoc

m100_Mux_Inverter1.SchDoc
m100_Mux_Inverter1.SchDoc

m100_PowerVoltage_Monitoring.SchDoc
m100_PowerVoltage_Monitoring.SchDoc

m100_Mux_Inverter2.SchDoc
m100_Mux_Inverter2.SchDoc

m100_Mux_Inverter3.SchDoc
m100_Mux_Inverter3.SchDoc

m100_Mux_Inverter4.SchDoc
m100_Mux_Inverter4.SchDoc

m100_Mux_Inverter5.SchDoc
m100_Mux_Inverter5.SchDoc

m100_Mux_Follower6.SchDoc
m100_Mux_Follower6.SchDoc

m100_Mux_Follower7.SchDoc
m100_Mux_Follower7.SchDoc

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Power Conversion

m100_Power_Conversion.SchDoc
m100_Power_Conversion.SchDoc

m100_GateDrive_Left.SchDoc
m100_GateDrive_Left.SchDoc

m100_BypassMosfet_Control.SchDoc
m100_BypassMosfet_Control.SchDoc

m100_GatePwr_Management.SchDoc
m100_GatePwr_Management.SchDoc

m100_GateDrive_Right.SchDoc
m100_GateDrive_Right.SchDoc

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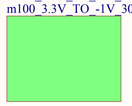
Date: 11/30/2020	Time: 12:12:21 PM	Sheet 1 of	This material is provided "As Is", without warranty of any kind, express or implied.
File: C:\Users\glenn\Documents\GWI\gwi_Dev\iNet-4xx 2004 Design\i4xx schematics\m100_Ma2SolarPCB\m100_SchPcb_CurrentWorkingFiles\Schematics\m100 Specific\m100_Group_Power_Conversion.SchDoc			

Power Supplies

m100_3.3V_TO_-1V_30mA_PowerSupply.SchDoc
m100_3.3V_TO_-1V_30mA_PowerSupply.SchDoc



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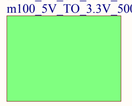

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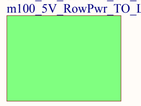

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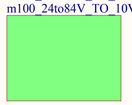

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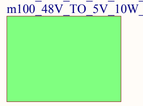

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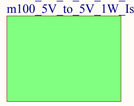

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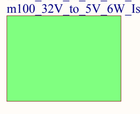

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System

m100_Xmc_uProc_ADC.SchDoc
m100_Xmc_uProc_ADC.SchDoc

m100_FPGA_System.SchDoc
m100_FPGA_System.SchDoc

m100_Xmc_uProc_IO.SchDoc
m100_Xmc_uProc_IO.SchDoc

m100_FPGA_Vmeasure.SchDoc
m100_FPGA_Vmeasure.SchDoc

m100_Xmc_uProc_System.SchDoc
m100_Xmc_uProc_System.SchDoc

m100_FPGA_Power.SchDoc
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